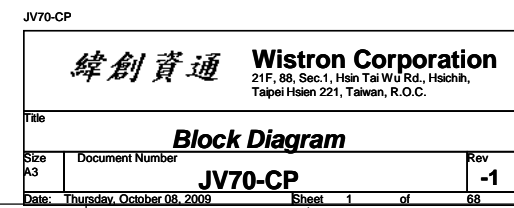


## PCB STACKUP

| MAXIM CHARGER<br>ISL88731A |           |
|----------------------------|-----------|
| INPUTS                     | OUTPUTS   |
| DCBATOUT                   | BT+<br>51 |



PCH Strapping

| Name                  | Schematics Notes   |
|-----------------------|--|
| SPKR                  | Reboot option at power-up<br>Default Mode: Internal weak Pull-down.<br>No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.  |
| INIT3_3V#             | Weak internal pull-down. Do not pull high.   |
| GNT3#/GPIO55          | Default Mode: Internal pull-up.<br>Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).  |
| INTVRMEN              | High (1) = Integrated VRM is enabled<br>Low (0) = Integrated VRM is disabled   |
| GNT0#, GNT1#          | Default (SPI): Left both GNT0# and GNT1# floating. No pull up required.<br>Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.<br>Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. |
| GNT2#/GPIO53          | Default - Internal pull-up.<br>Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).   |
| GPIO33                | Default: Do not pull low.<br>Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.   |
| SPI_MOSI              | Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor<br>Disable iTPM: Left floating, no pull-down required.  |
| NV_ALE                | Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.<br>Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.  |
| NC_CLE                | Weak internal pull-up. Do not pull low.  |
| HAD_DOCK_EN#/GPIO[33] | Low (0): Flash Descriptor Security will be overridden.<br>High (1) : Flash Descriptor Security will be in effect.  |
| HDA_SDO               | Weak internal pull-down. Do not pull high.   |
| HDA_SYNC              | Weak internal pull-down. Do not pull high.   |
| GPIO15                | Weak internal pull-down. Do not pull high.   |
| GPIO8                 | Weak internal pull-up. Do not pull low.  |
| GPIO27                | Default = Do not connect (floating)<br>High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.<br>Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.       |

PCIE Routing

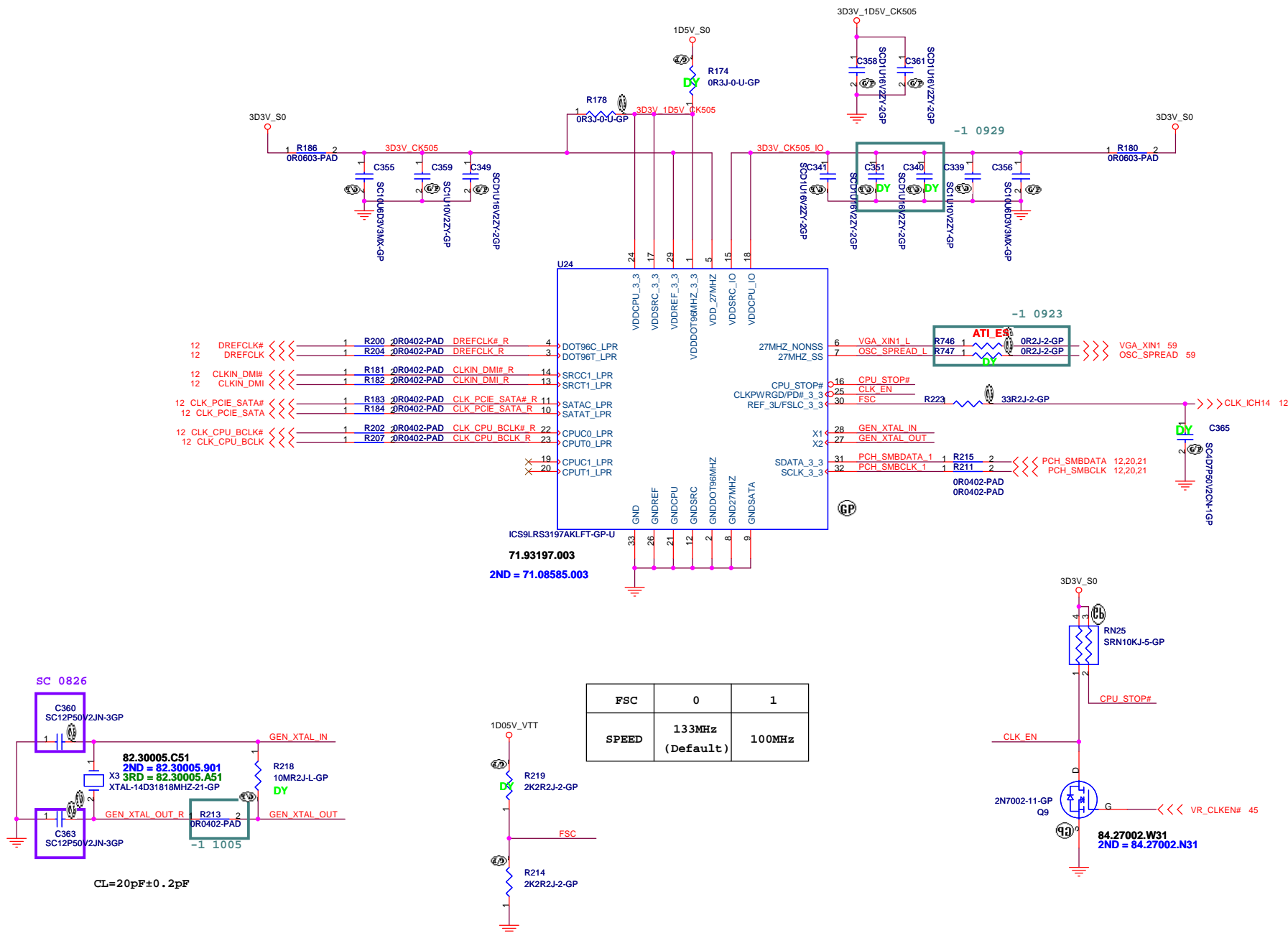
|       |               |
|-------|---------------|
| LANE1 | LAN           |
| LANE2 | MiniCard WLAN |
|       |               |

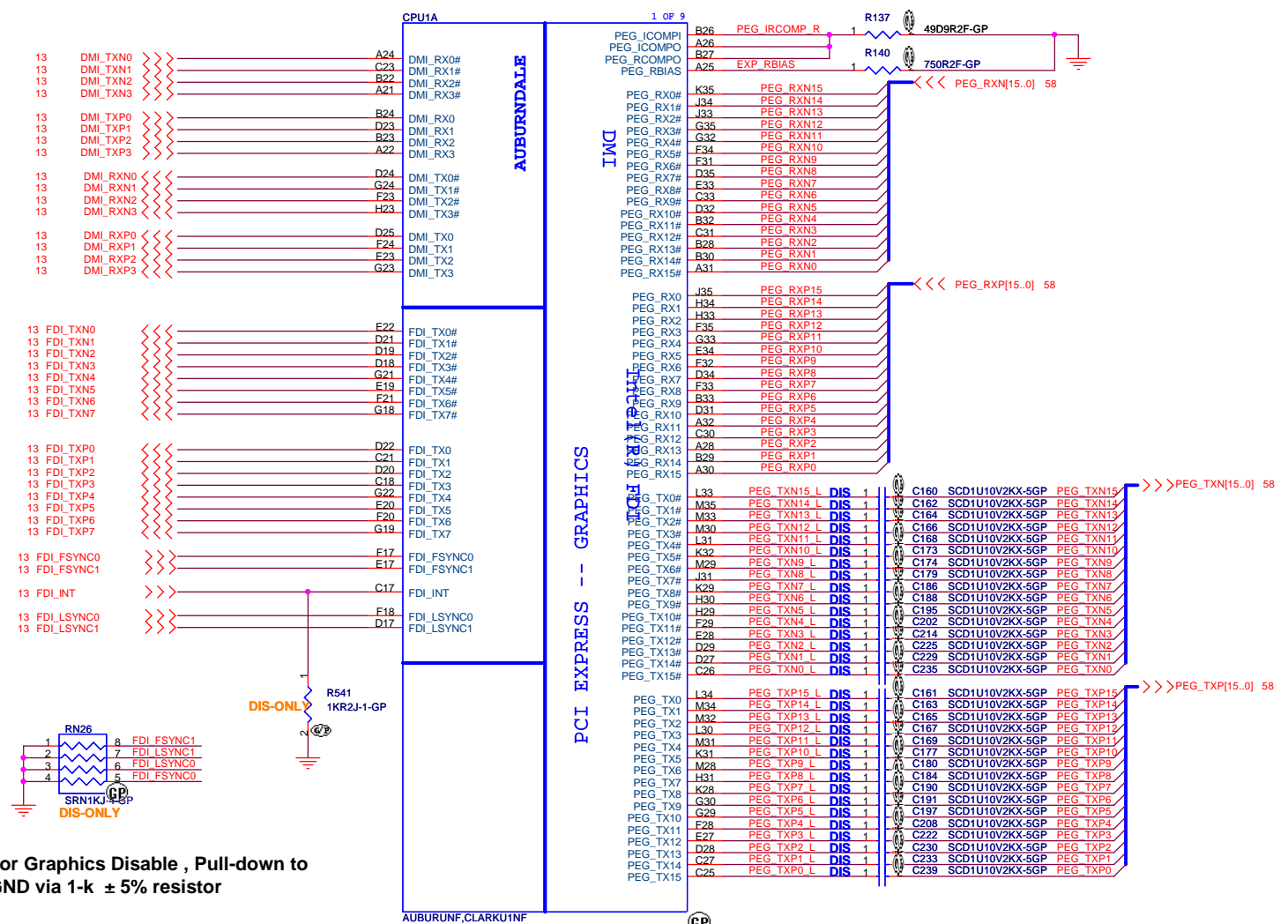
USB

| Pair | Device       |
|------|--------------|
| 0    | USB1         |
| 1    | USB2         |
| 2    | USB4         |
| 3    | MINICARD1    |
| 4    | WECAM        |
| 5    | NC           |
| 6    | NC           |
| 7    | NC           |
| 8    | NC           |
| 9    | USB3(HS)     |
| 10   | Finger Print |
| 11   | Blue Tooth   |
| 12   | NC           |
| 13   | Cardreader   |

Processor Strapping

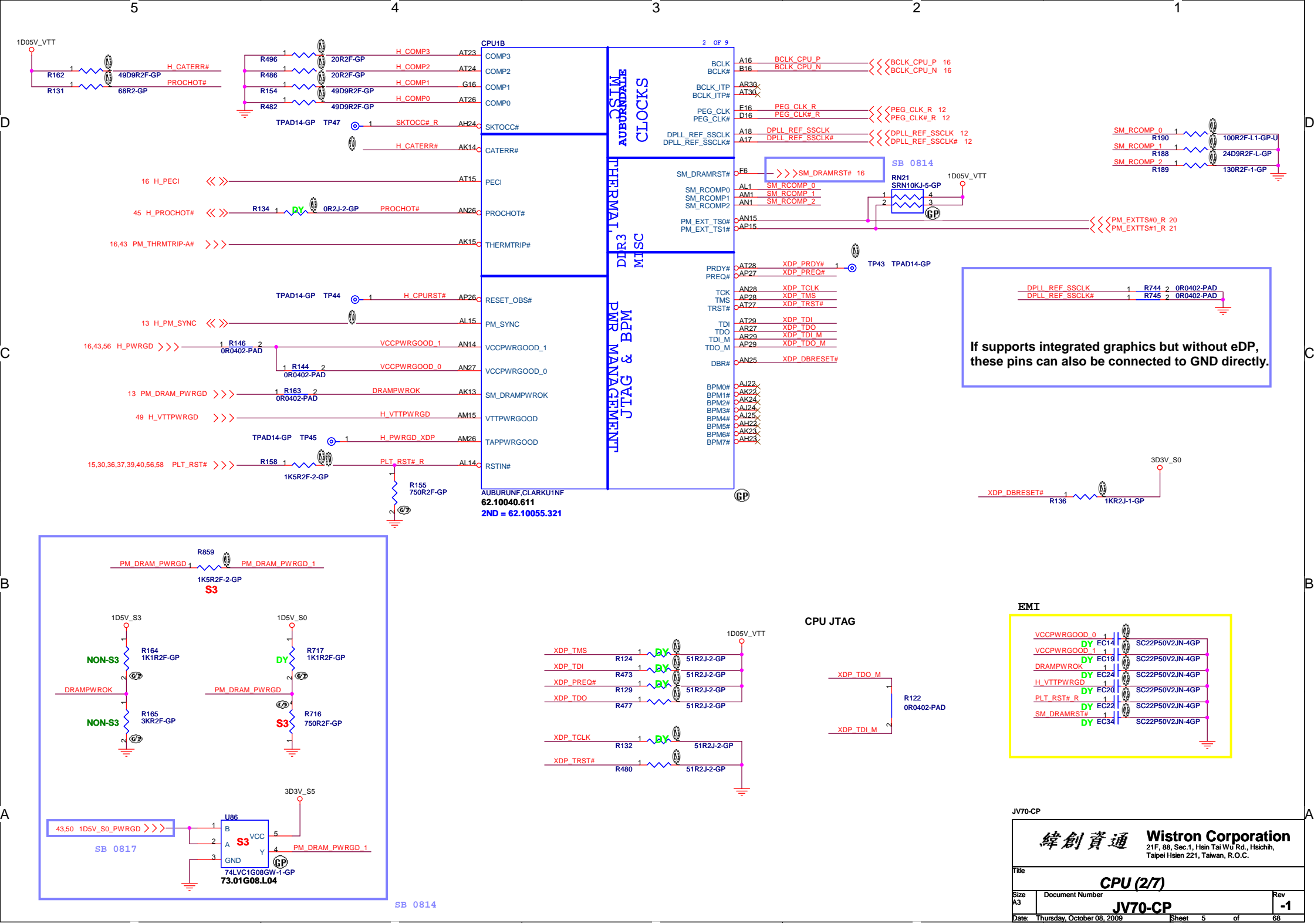
| Pin Name | Strap Description  | Configuration (Default value for each bit is 1 unless specified otherwise)  | Default Value |
|----------|--|---|---------------|
| CFG[4]   | Embedded DisplayPort Presence                              | 1: Disabled - No Physical Display Port attached to Embedded DisplayPort.<br>0: Enabled - An external Display Port device is connected to the Embedded Display Port.   | 1             |
| CFG[3]   | PCI-Express Static Lane Reversal                           | 1: Normal Operation.<br>0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...  | 1             |
| CFG[0]   | PCI-Express Configuration Select                           | 1: Single PCI-Express Graphics<br>0: Bifurcation enabled  | 1             |
| CFG[7]   | Reserved - Temporarily used for early Clarksfield samples. | Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor<br>Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality. | 0             |

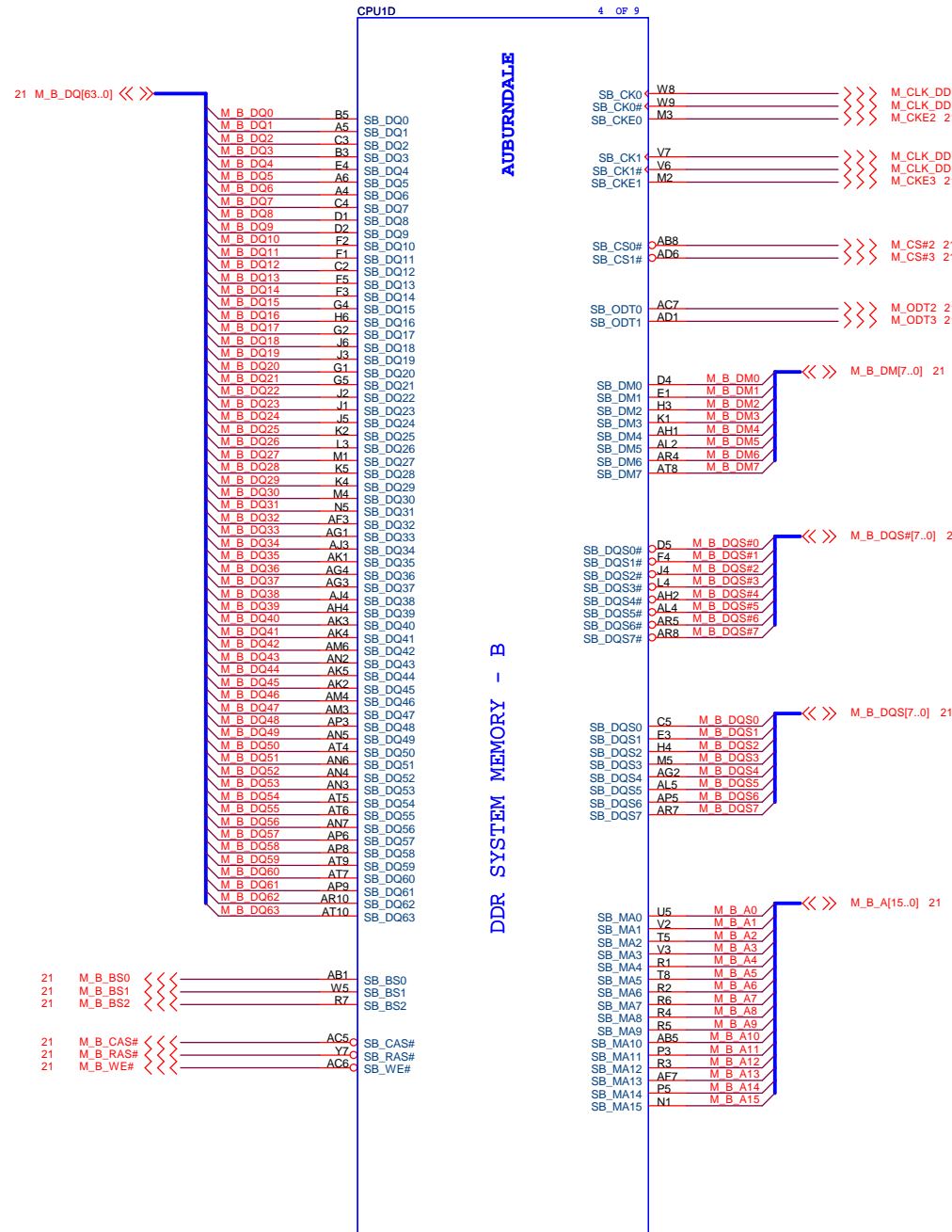
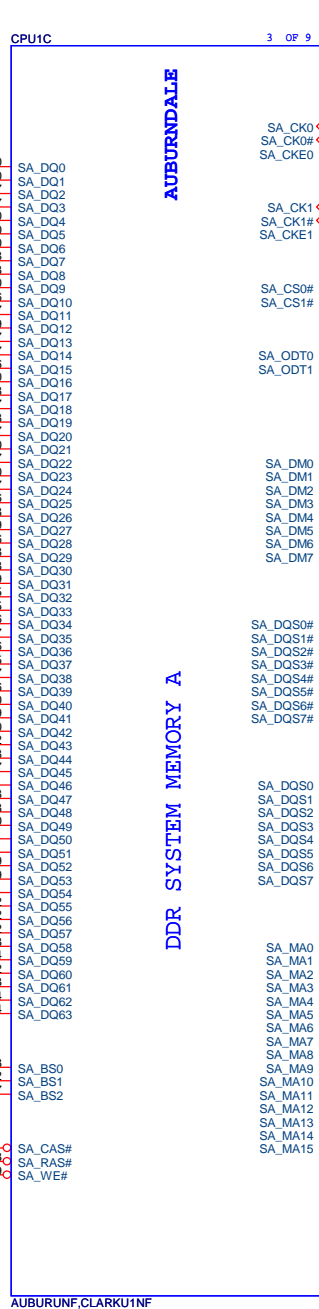




JV70-CP

|  |                 |
|--|-----------------|
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| Title  |                 |
| <b>CPU (1/7)</b>   |                 |
| Size   | Document Number |
| A3   | <b>JV70-CP</b>  |
| Date: Thursday, October 08, 2009   | Sheet 4 of 68   |
| Rev -1   |                 |





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Title CPU (3/7)  
Size A3 Document Number JV70-CP Rev -1  
Date: Thursday, October 08, 2009 Sheet 6 of 68

VCC\_CORE

-1 0929

### PROCESSOR CORE POWER

65A

VCC\_CORE

CPU1F

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

AUBURUNF.CLARKU1NF  
62.10040.611  
2ND = 62.10055.321

6 OF 9

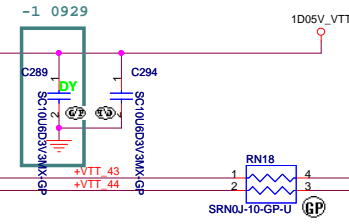
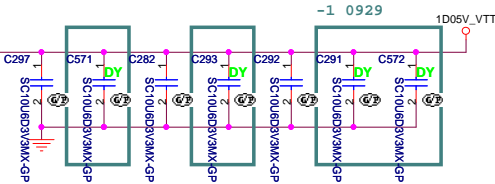


VTT0 AH14  
VTT0 AH12  
VTT0 AH11  
VTT0 AH10  
VTT0 J14  
VTT0 J13  
VTT0 H14  
VTT0 H12  
VTT0 G14  
VTT0 G13  
VTT0 G12  
VTT0 G11  
VTT0 F14  
VTT0 F13  
VTT0 F12  
VTT0 F11  
VTT0 E14  
VTT0 E12  
VTT0 D14  
VTT0 D13  
VTT0 D12  
VTT0 D11  
VTT0 C14  
VTT0 C13  
VTT0 C12  
VTT0 C11  
VTT0 B14  
VTT0 B12  
VTT0 A14  
VTT0 A13  
VTT0 A12  
VTT0 A11

VTT0 AF10  
VTT0 AE10  
VTT0 AC10  
VTT0 AB10  
VTT0 Y10  
VTT0 W10  
VTT0 U10  
VTT0 T10  
VTT0 J12  
VTT0 J11  
VTT0 J16  
VTT0 J15

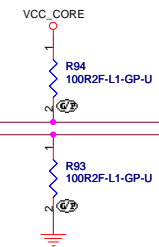
PSI# >AN33 >>> PSI# 45  
AK35 H\_VID0 >>> H\_VID[6..0] 45  
AK33 H\_VID1  
AK34 H\_VID2  
AL35 H\_VID3  
AL33 H\_VID4  
AM33 H\_VID5  
AM35 H\_VID6  
AM34 >>> PM\_DPRSLPVR 45  
G15 H\_VTTVID1 >>> H\_VTTVID1 49  
Clarksfield H\_VTTVID1 = Low, VTT = 1.1V  
Arrandale H\_VTTVID1 = High, VTT = 1.05V

ISENSE >AN35 <<< IMVP\_IMON 45  
VCC\_SENSE >AJ34 >>> VCC\_SENSE 45  
>AJ35 >>> VSS\_SENSE 45  
VTT\_SENSE >B15 >>> VTT\_SENSE 49  
>A15 >>> TP VSS\_SENSE\_VTT 1  
TP90 TPAD14-GP



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



JV70-CP

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Title  
**CPU (4/7)**

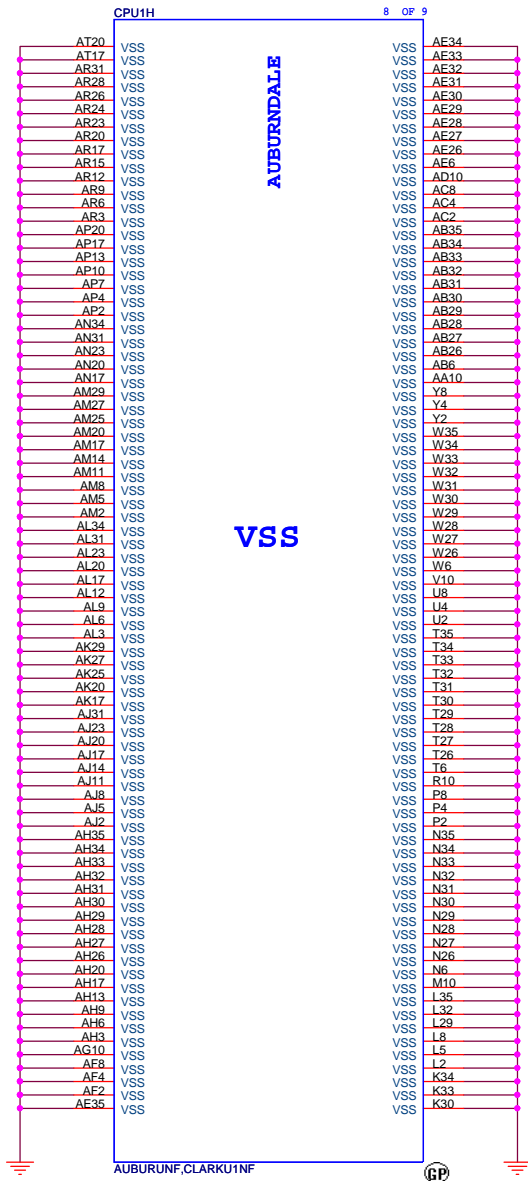
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|--------|-----------------|-----------|
| Size   | Document Number | Rev       |
| Custom | <b>JV70-CP</b>  | <b>-1</b> |

Date: Thursday, October 08, 2009 Sheet 7 of 68

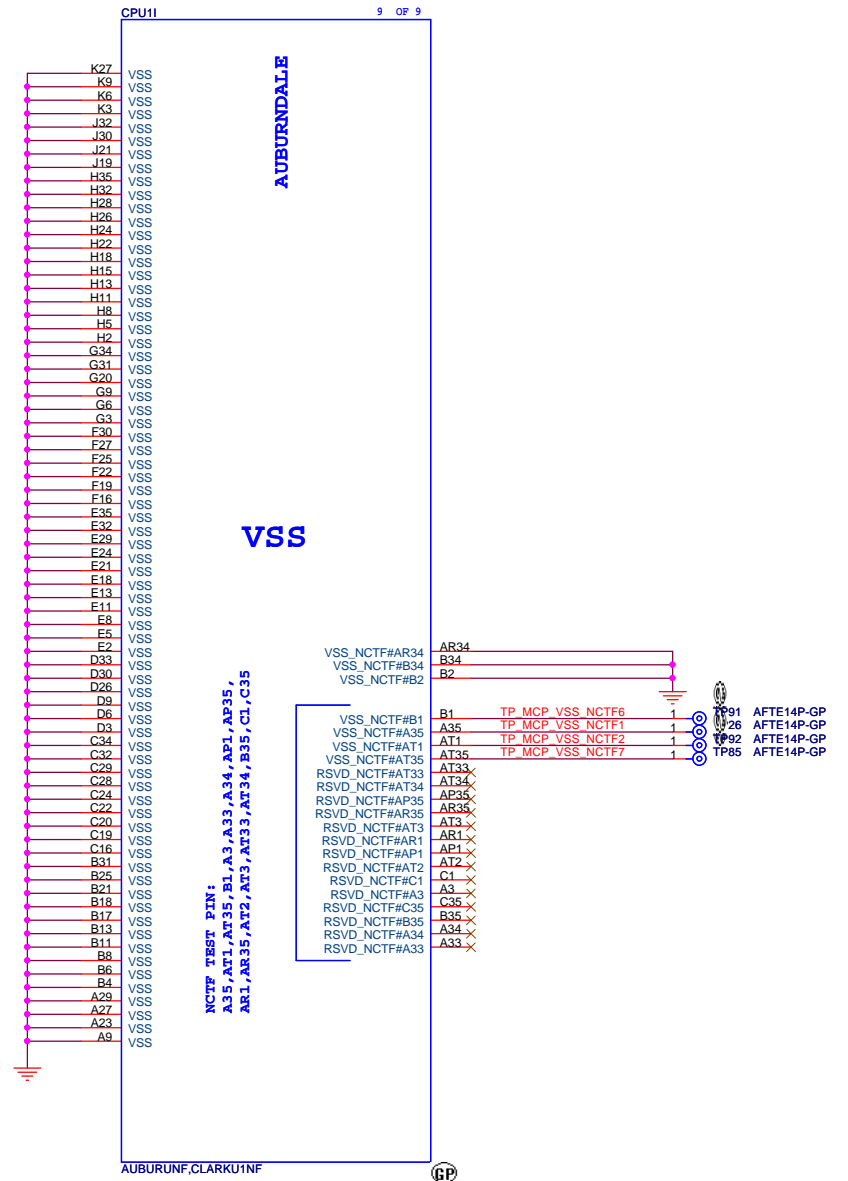








62.10040.611  
2ND = 62.10055.321

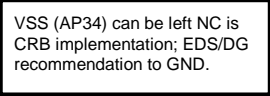


62.10040.611  
2ND = 62.10055.321

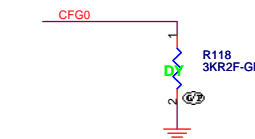
JV70-CP

|  |                 |     |
|--|-----------------|-----|
| 緯創資通 Wistron Corporation   |                 |     |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                 |     |
| Title  |                 |     |
| CPU (6/7)  |                 |     |
| Size   | Document Number | Rev |
| A3   | JV70-CP         | -1  |
| Date: Thursday, October 08, 2009   | Sheet 9 of 68   |     |

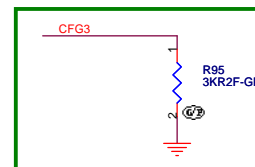
Diagram of the SB 0814 component showing its internal structure and connections. The component is labeled "SB 0814" at the bottom. It contains a block labeled "20 SA\_DIMM\_VREF# 21 SB\_DIMM\_VREF#" with two wavy lines representing signals. These signals connect to a block labeled "RN15" (a resistor network) and "SRN0J-10-GP-U" (a transformer). The "RN15" block is connected to "DY" (a diode) and "GP" (a ground symbol). The "SRN0J-10-GP-U" block is connected to "H RSV9" and "H RSV10".



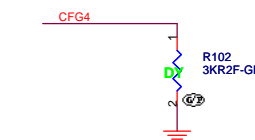
| PCI-Express Configuration Select |                                       |
|----------------------------------|---------------------------------------|
| CFG0                             | 1:Single PEG<br>0:Bifurcation enabled |



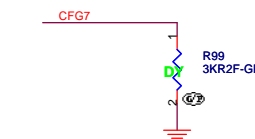
| CFG3 - PCI-Express Static Lane Reversal |  |
|---|--|
| CFG3                                    | 1 : Normal Operation<br>0 : Lane Numbers Reversed<br>15 -> 0, 14 -> 1, ... |



| CFG4 - Display Port Presence |  |
|------------------------------|--|
| CFG4                         | 1:Disabled; No Physical Display Port attached to Embedded Display Port<br>0:Enabled; An external Display Port device is connected to the Embedded Display Port |



|  |  |
|--|--|
| CFG7(Reserved) - Temporarily used for early Clarksfield samples. |  |
| CFG7   | <p>Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.</p> <p>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].</p> <p>For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.</p> |





LAN

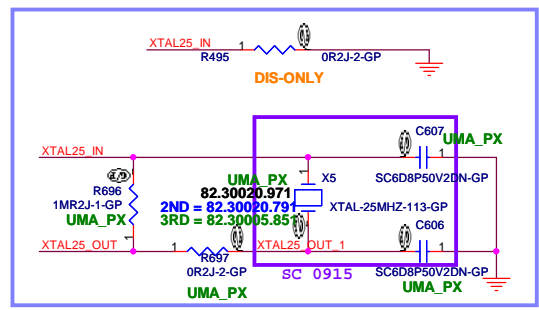
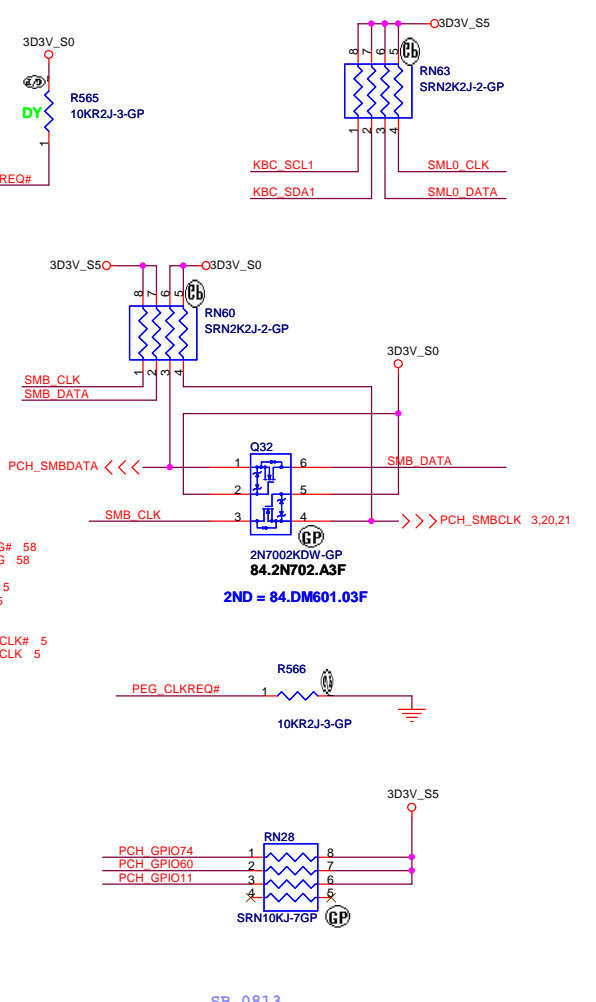
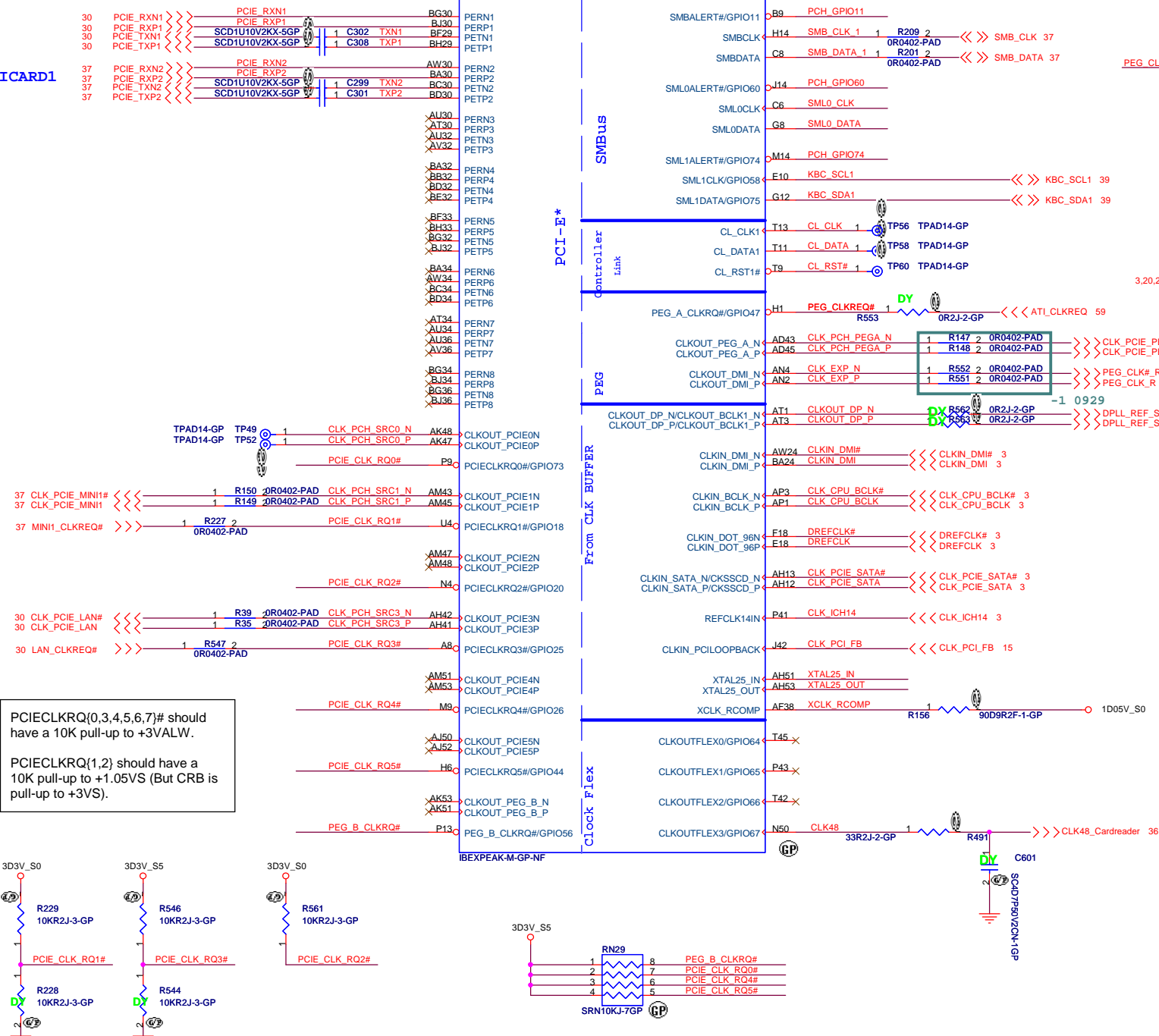
MINICARD1

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

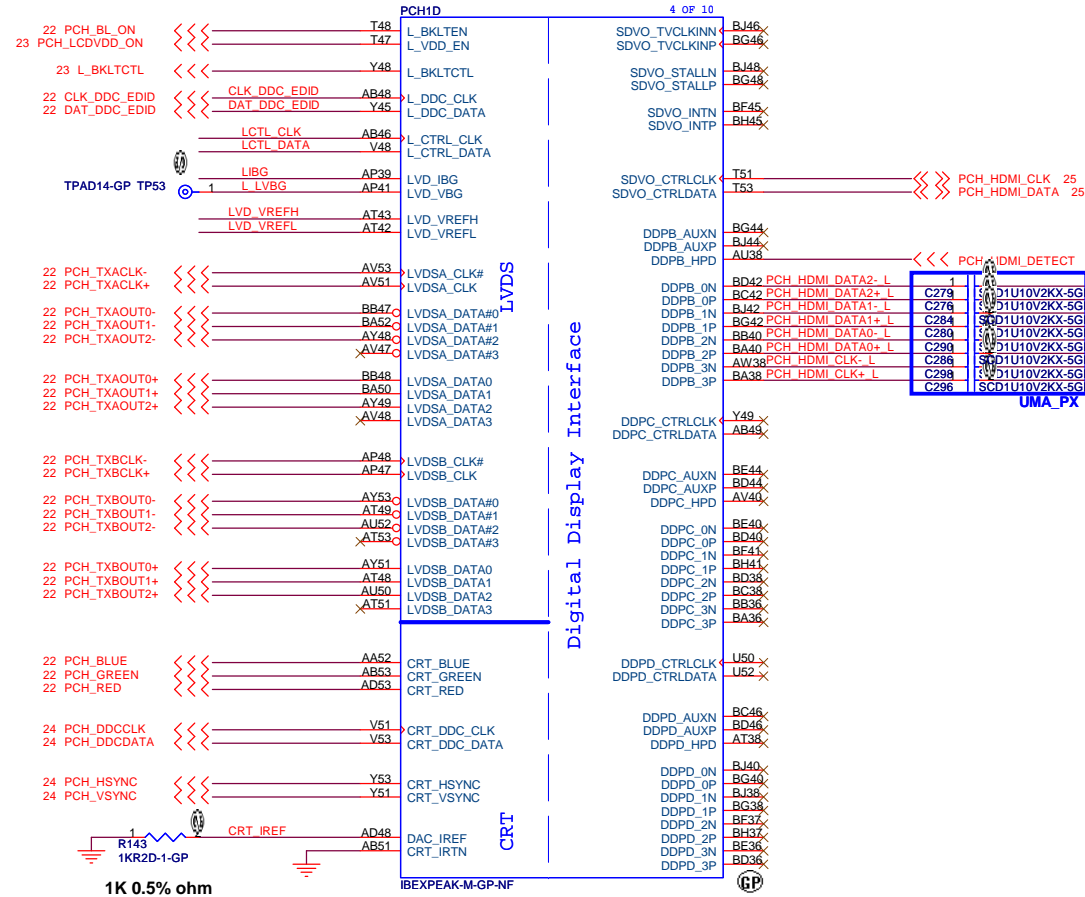
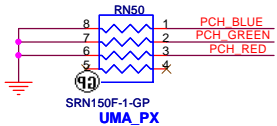
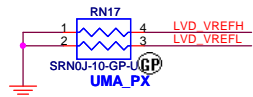
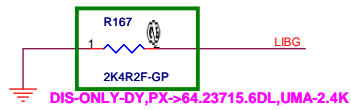
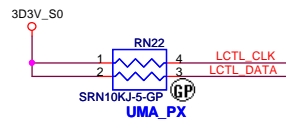
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

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PCH18 2 OF 10







JV70-CP

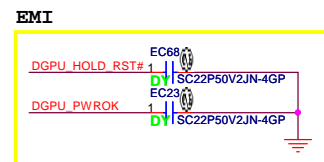
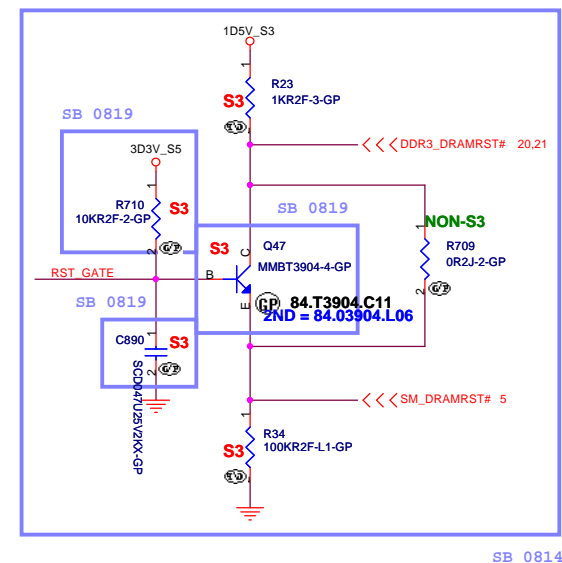
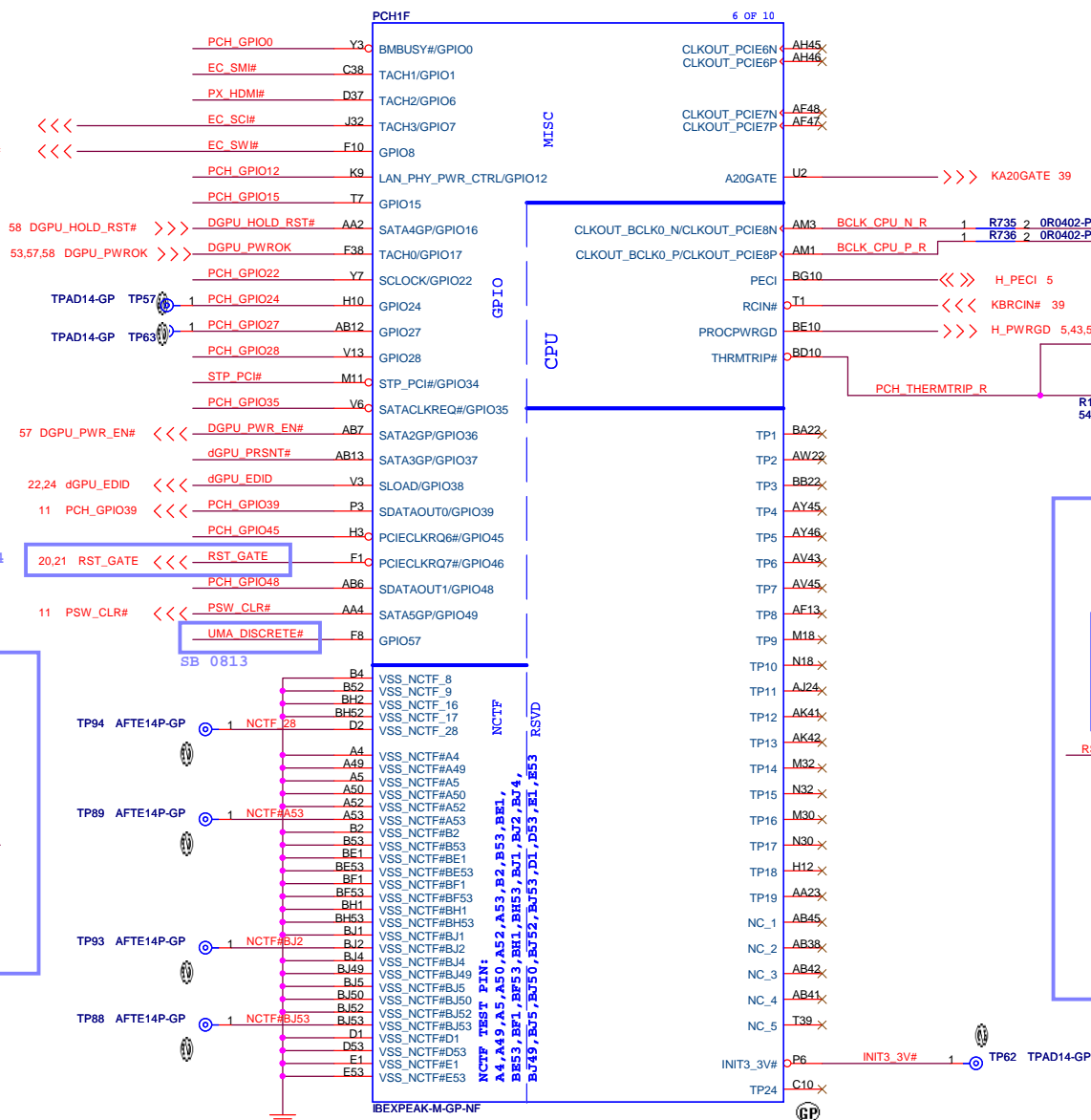
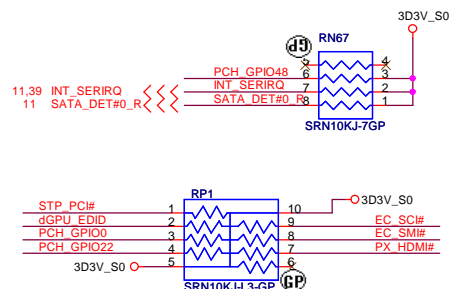
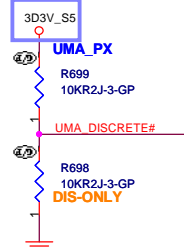
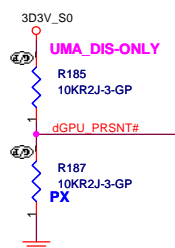
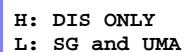
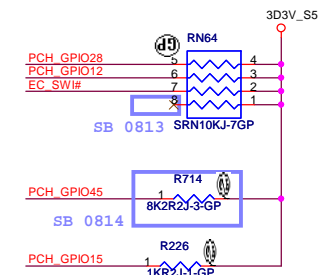
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|       |                            |         |           |       |
|-------|----------------------------|---------|-----------|-------|
| Title |                            |         | PCH (4/9) |       |
| Size  | Document Number            | JV70-CP |           | Rev   |
| A3    |                            |         |           | -1    |
| Date: | Thursday, October 08, 2009 | Sheet   | 14        | of 68 |

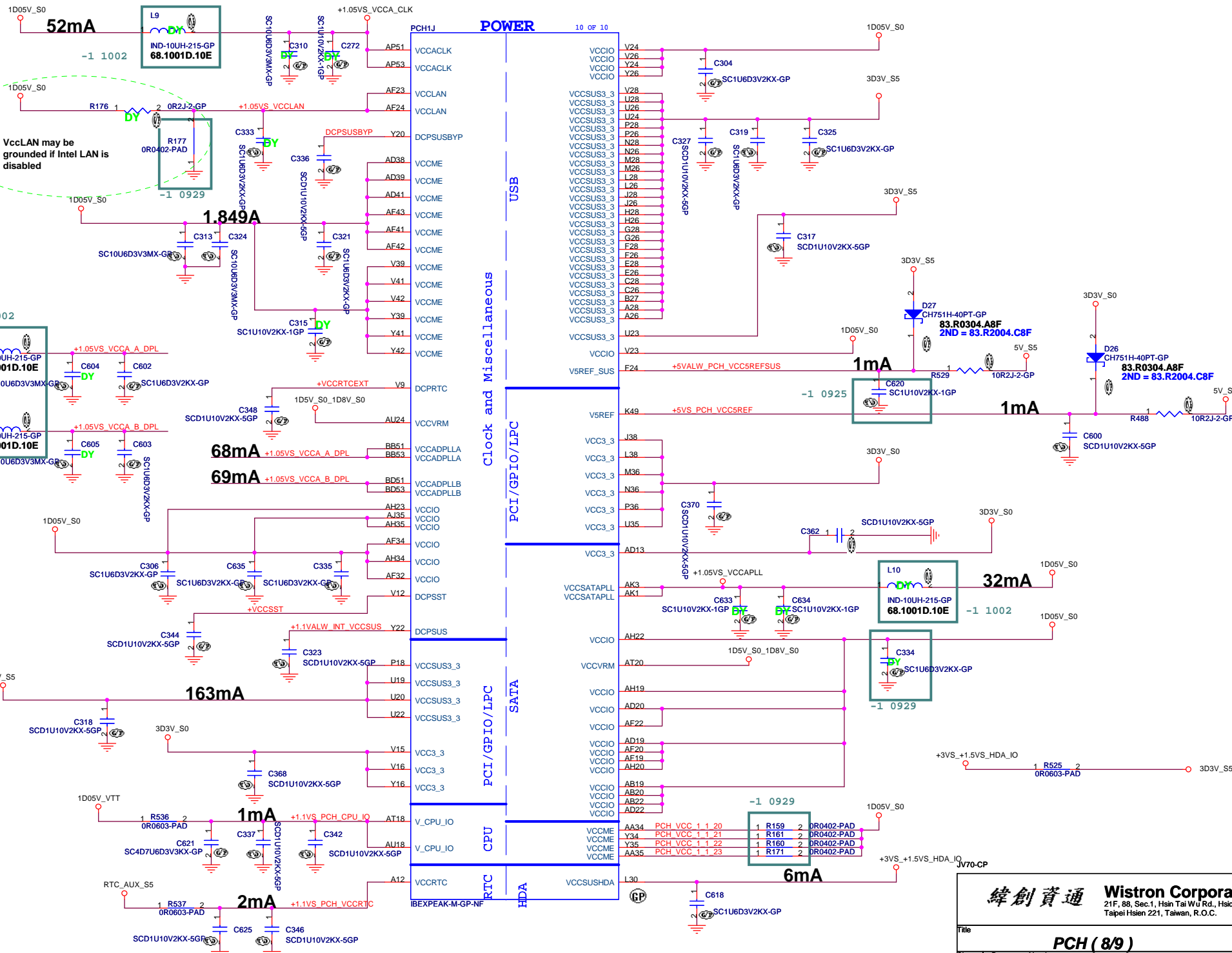




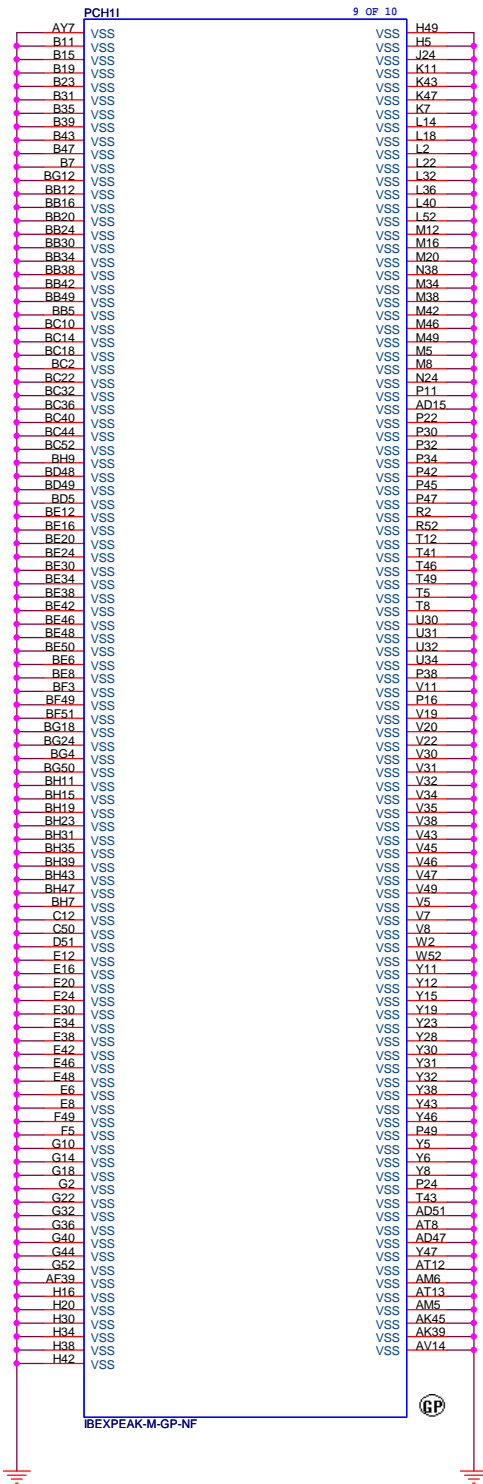
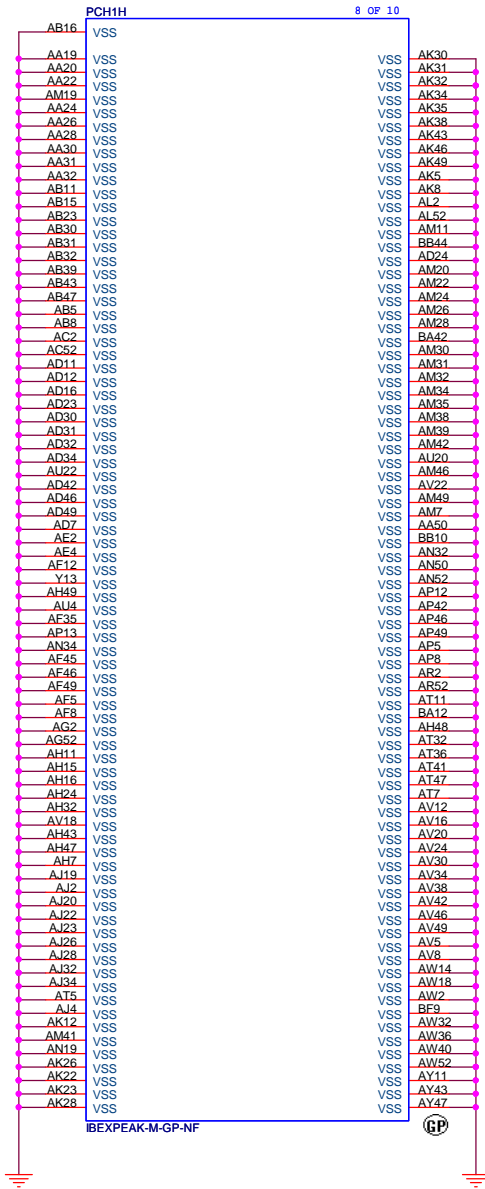
GPIO27 has a weak[20K] internal pull up.  
To enable on-die PLL Voltage regulator,  
should not place external pull down.







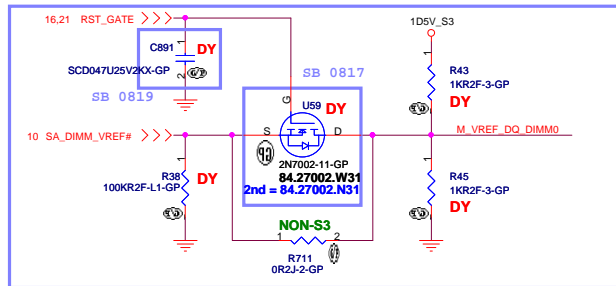
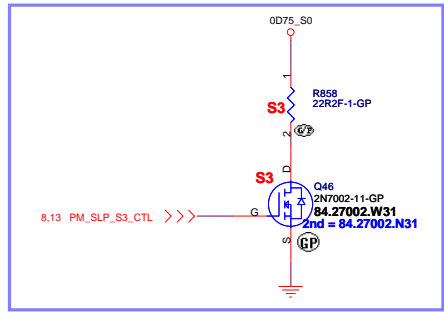
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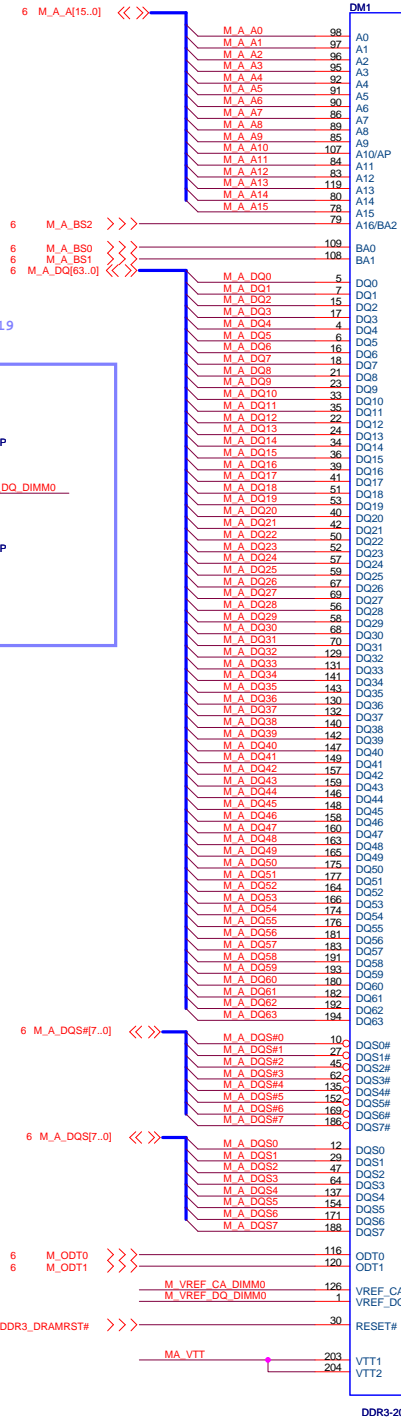
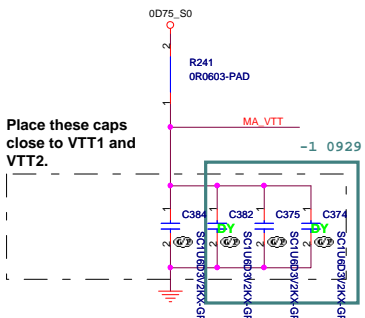
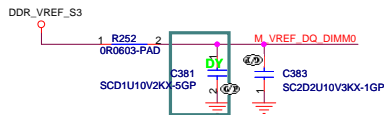
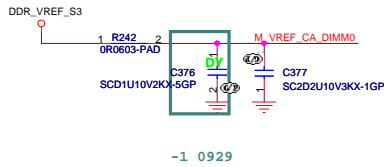
JV70-CP

|       |                            |             |          |
|-------|----------------------------|-------------|----------|
| Title |                            | PCH ( 9/9 ) |          |
| Size  | Document Number            | Rev         |          |
| A3    | JV70-CP                    | -1          |          |
| Date: | Thursday, October 08, 2009 | Sheet       | 19 of 68 |

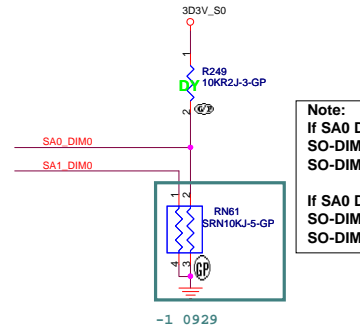
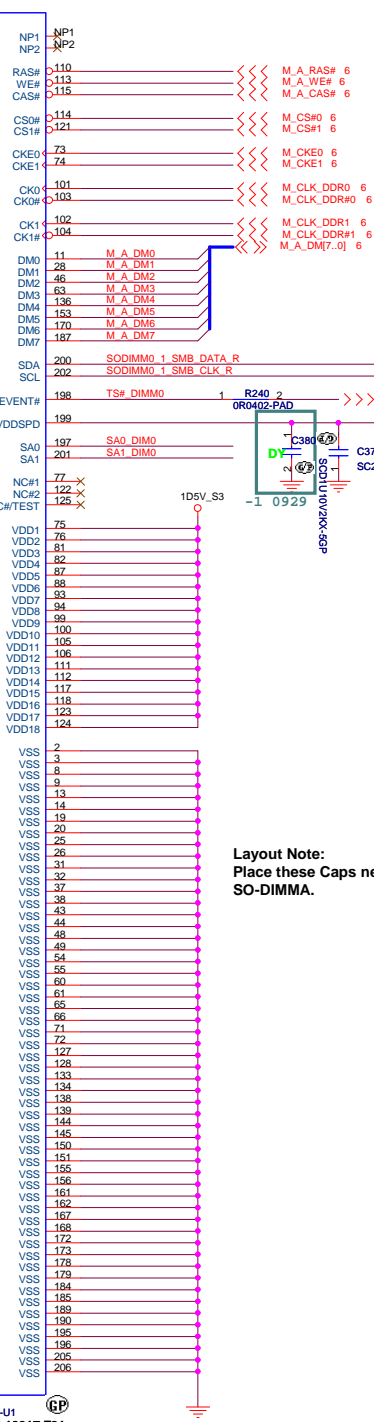
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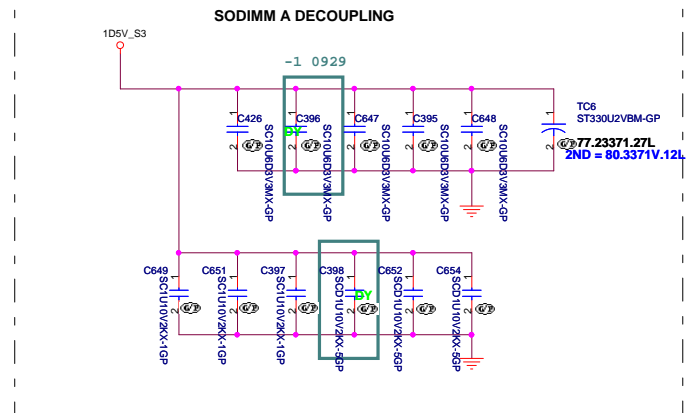
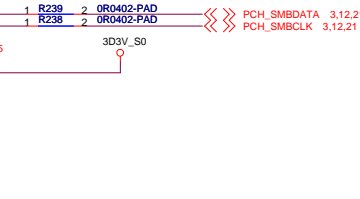
SB 0814



REVERSE TYPE



Note:  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
  
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

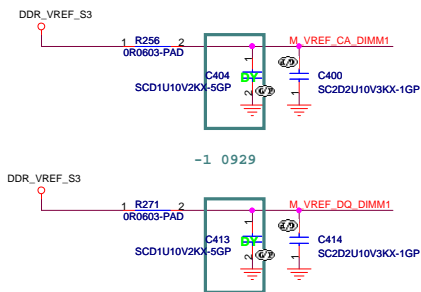
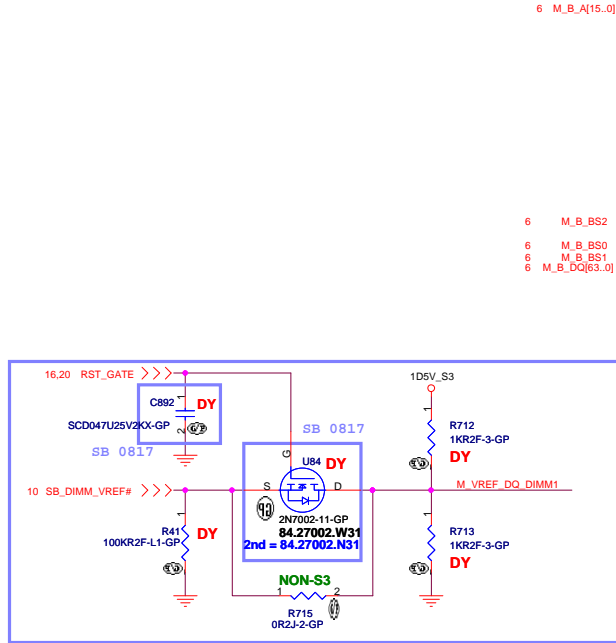


Layout Note:  
Place these Caps near  
SO-DIMMA.

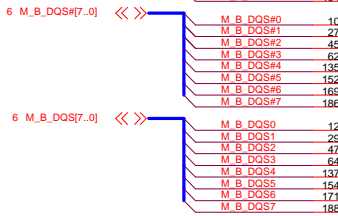
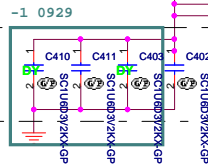
JV70-CP

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|      |                            |                |
|------|----------------------------|----------------|
| File | Document Number            | Rev            |
|      | DDRIII Socket DM1          |                |
| Size | Custom                     | -1             |
| Date | Thursday, October 08, 2009 | Sheet 20 of 68 |



Place these caps close to VTT1 and VTT2.



SO-DIMMB is placed farther from the Processor than SO-DIMMA

H = 5.2mm

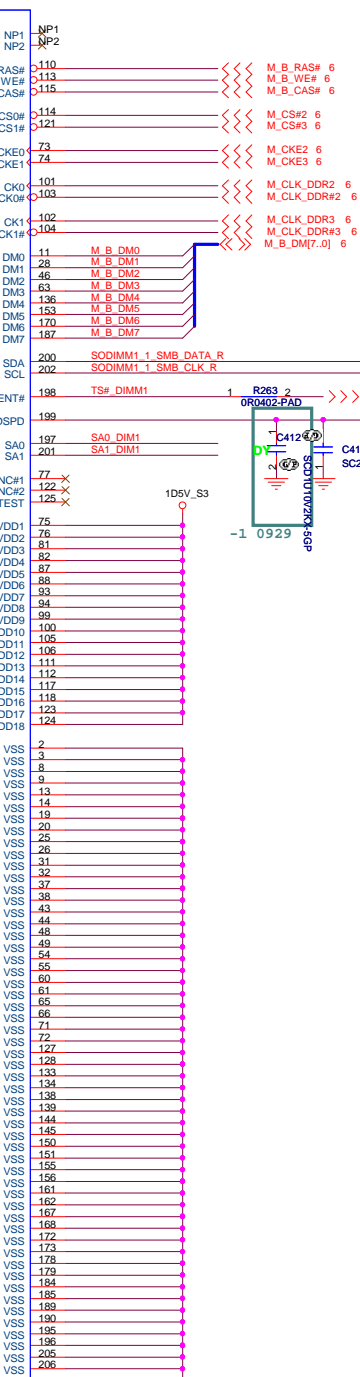
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62.10017.F81

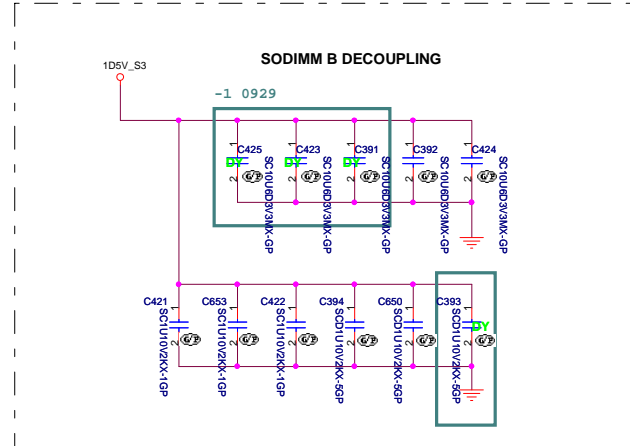
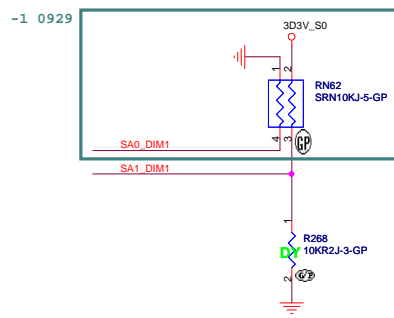
2ND = 62.10017.P41  
3RD = 62.10017.P61  
4TH = 62.10017.N41

BOM change to 62.10017.F81

REVERSE TYPE



Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

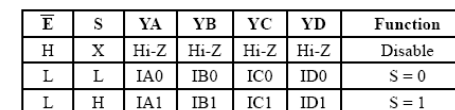
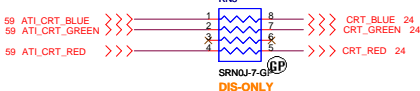
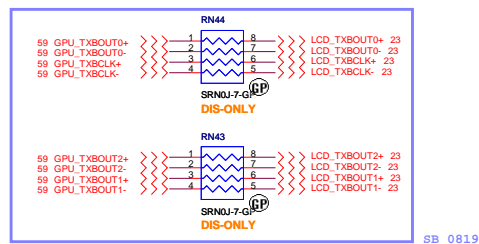
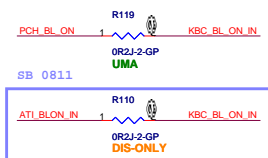


JV70-CP

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| DDR/III Socket DM2 |                            |                |
|--------------------|----------------------------|----------------|
| Size               | Document Number            | Rev            |
| Custom             | JV70-CP                    | -1             |
| Date:              | Thursday, October 08, 2009 | Sheet 21 of 68 |

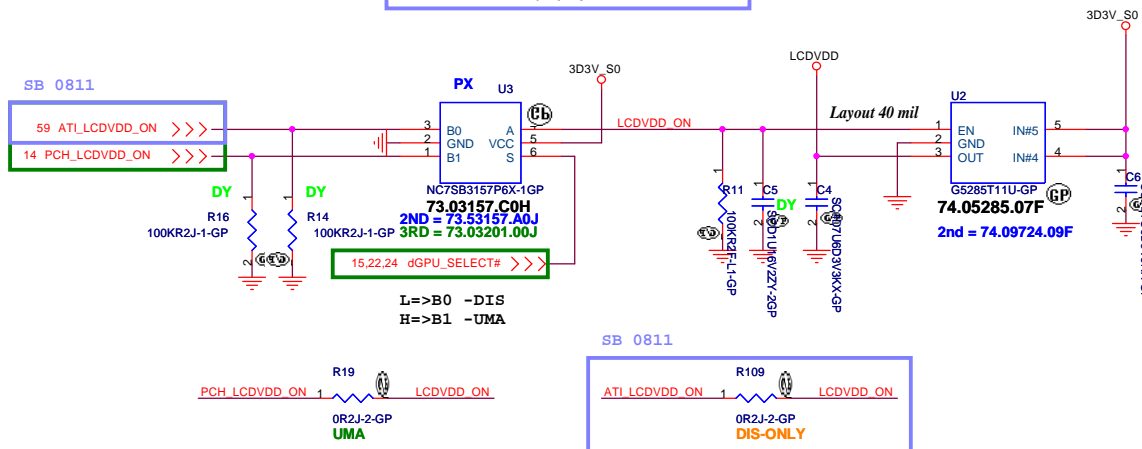
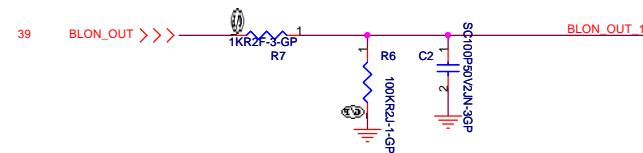
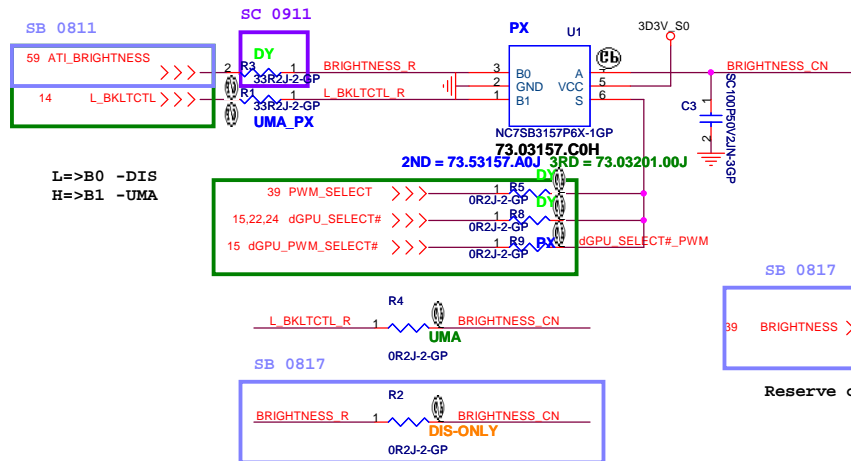
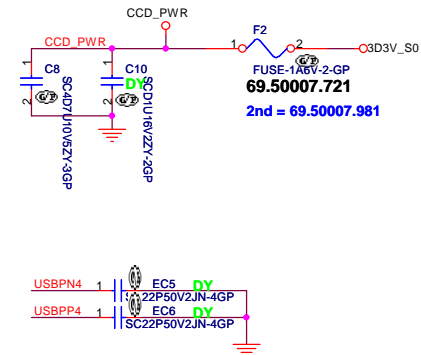
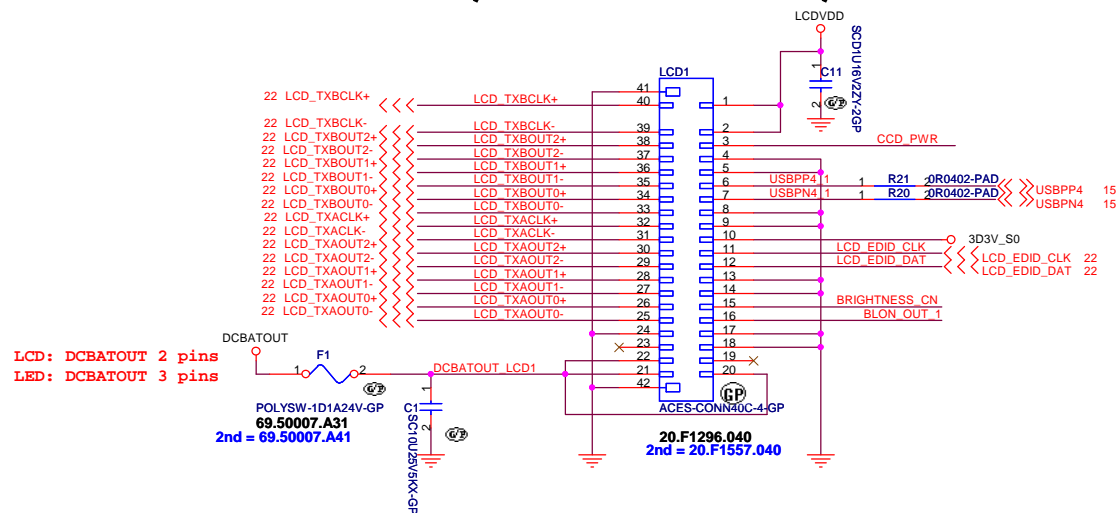




|                  |                            |       |          |
|------------------|----------------------------|-------|----------|
| Title            |                            |       |          |
| <b>PX SWITCH</b> |                            |       |          |
| Size             | Document Number            | Rev   |          |
| Custom           |                            | -1    |          |
| Date:            | Thursday, October 08, 2009 | Sheet | 22 of 68 |



## LCD/INVERTER/CCD CONN



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Title **LCD CONN**

| Size | Document Number |
|------|-----------------|
|------|-----------------|

**JV70-CP**

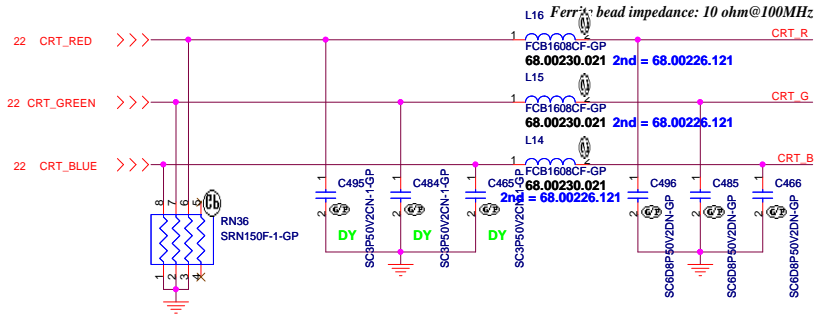
Date: Thursday, October 08, 2009

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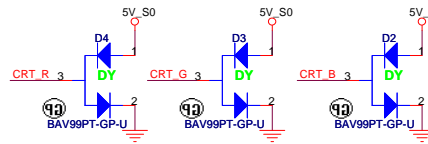
of

|     |    |
|-----|----|
| Rev | -1 |
|-----|----|

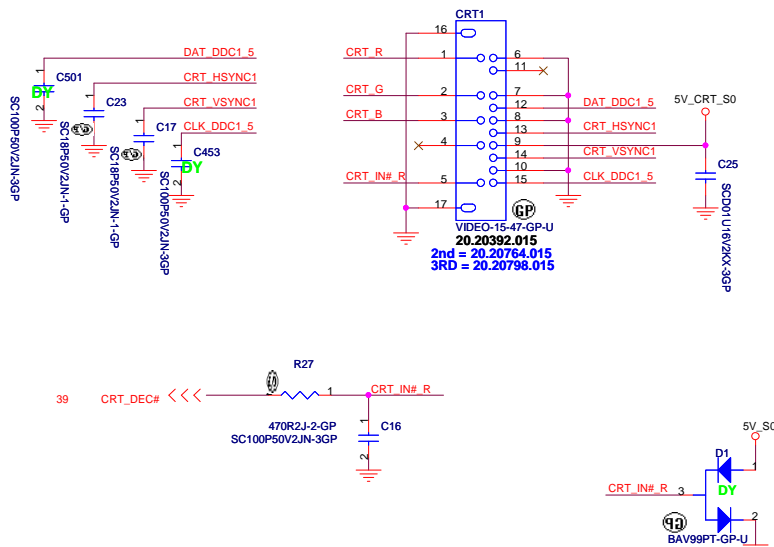
Layout Note:  
Place these resistors  
close to the CRT-out  
connector



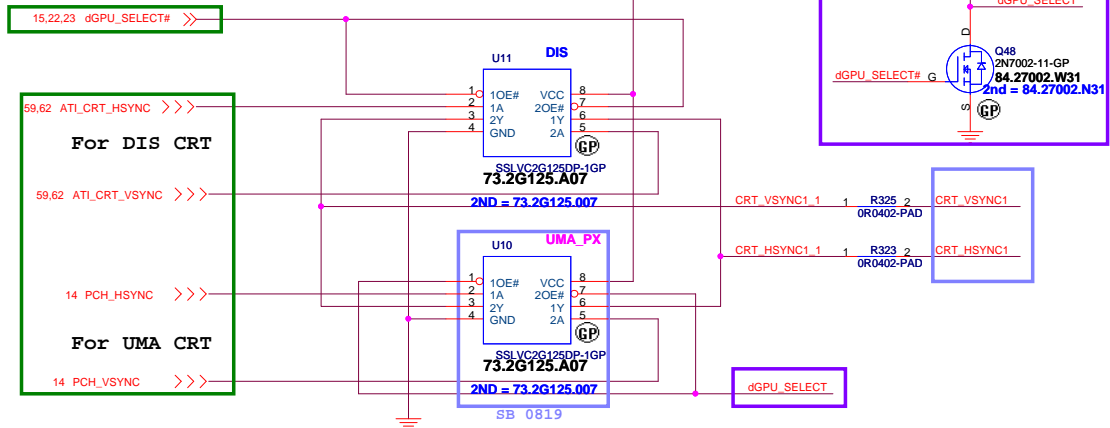
**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



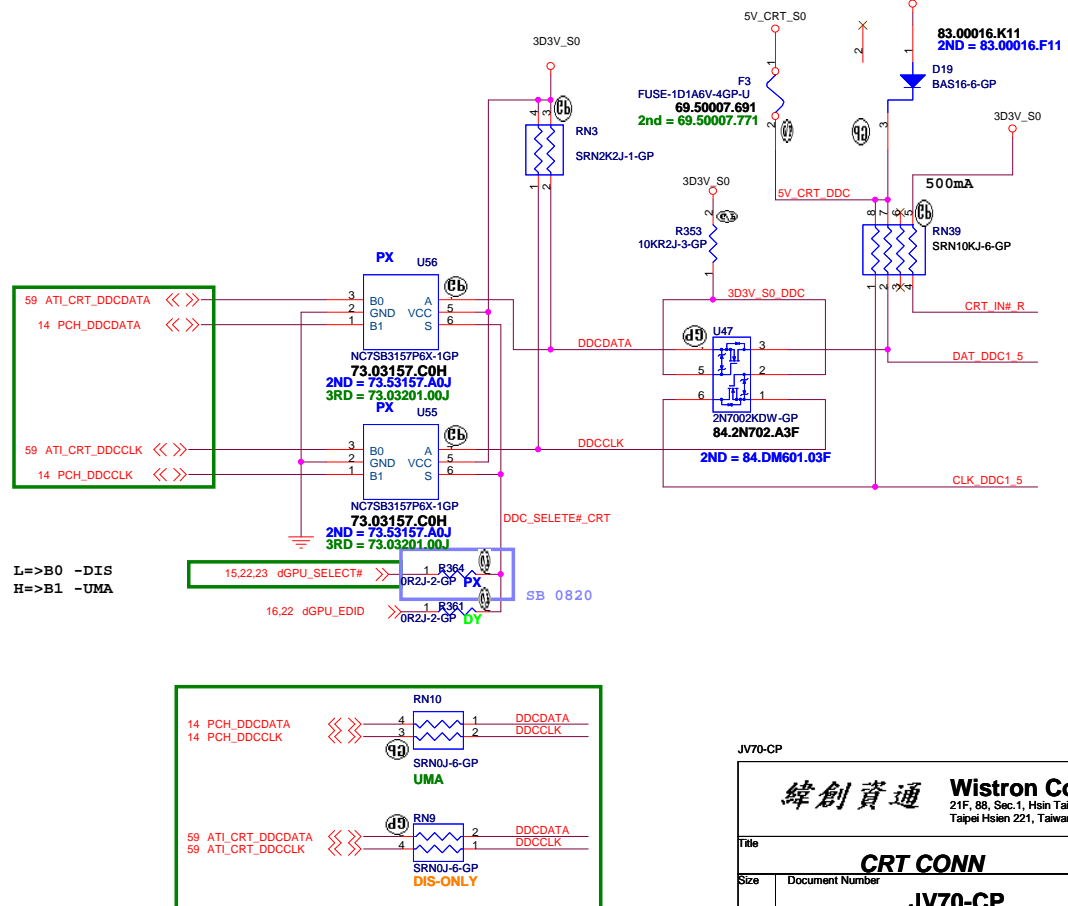
## CRT I/F & CONNECTOR



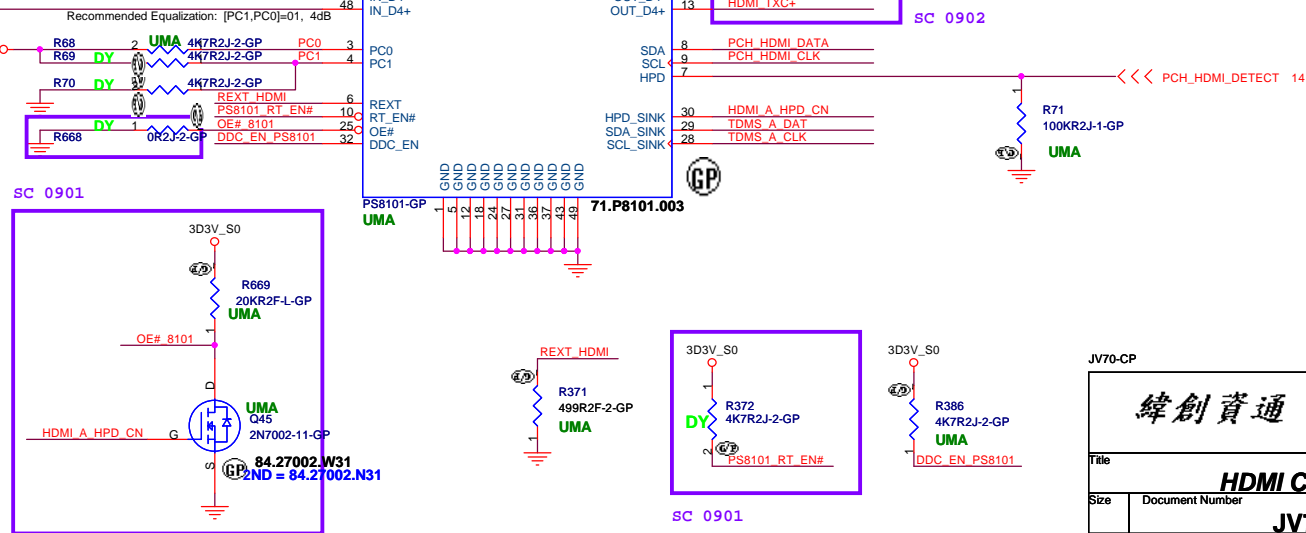
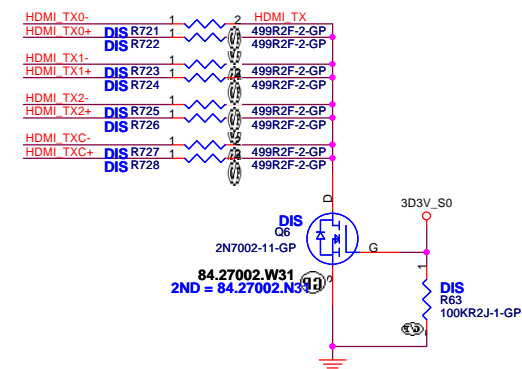
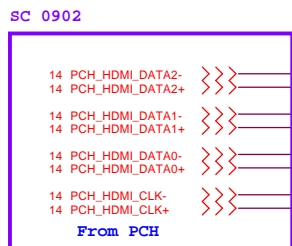
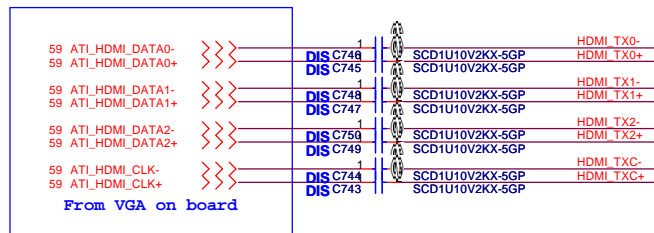
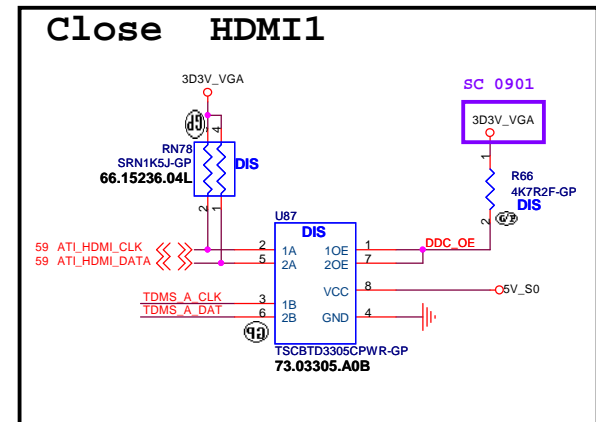
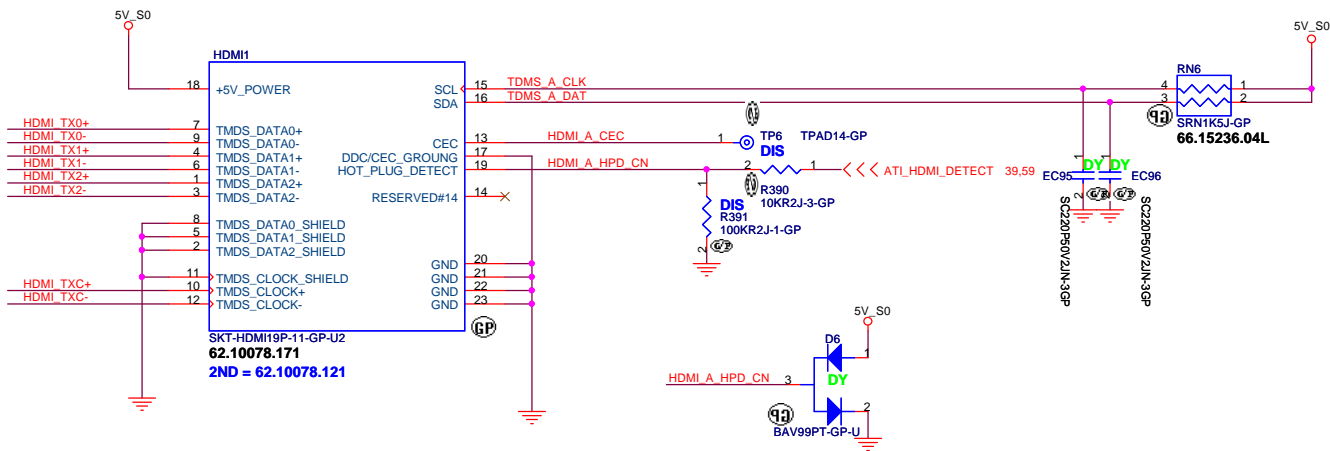
L=> DIS  
H=> UMA



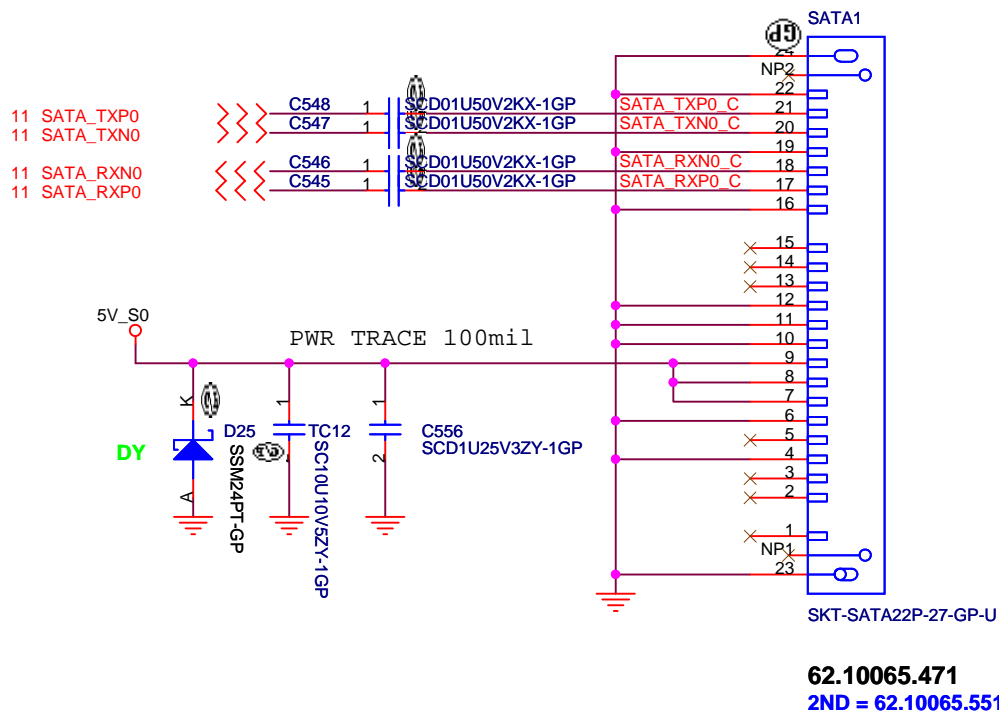
## DDC\_CLK & DATA level shift



L=>B0 -DIS  
H=>B1 -UMA



# SATA Connector



JV70-CP

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Title

HDD CONN

Size

Document Number

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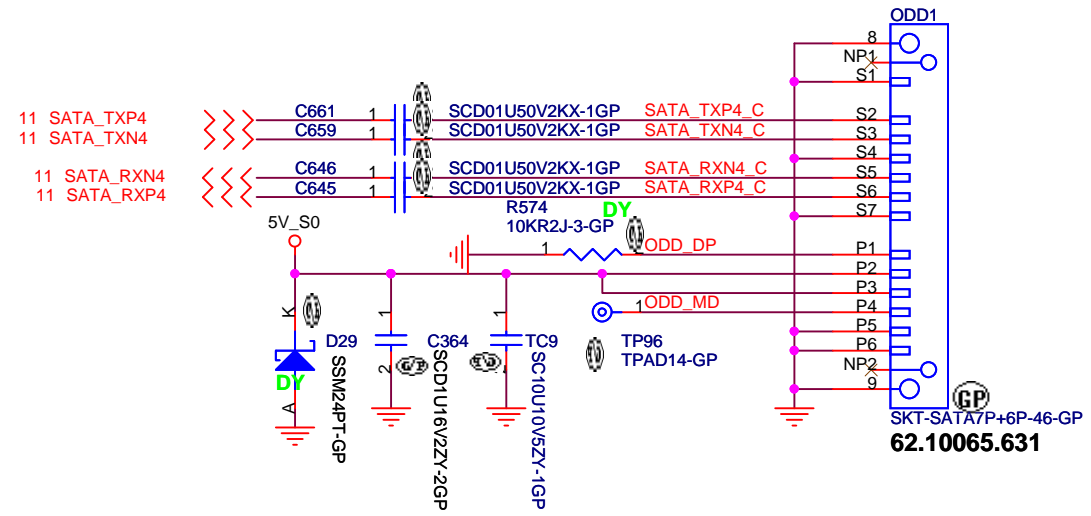
Rev

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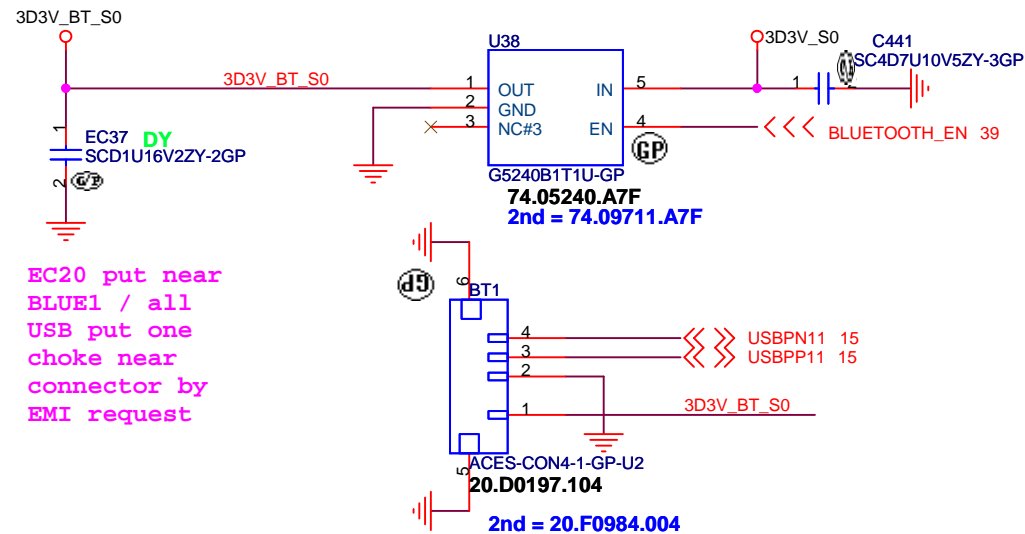
# ODD Connector



JV70-CP

|                                  |                 |  |     |
|----------------------------------|-----------------|--|-----|
| 緯創資通                             |                 | Wistron Corporation  |     |
|                                  |                 | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |     |
| Title                            |                 |  |     |
| ODD                              |                 |  |     |
| Size                             | Document Number |  | Rev |
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# BLUETOOTH MODULE



JV70-CP

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**BLUETOOTH**

Size

Document Number

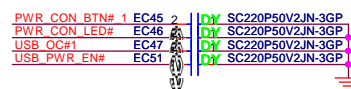
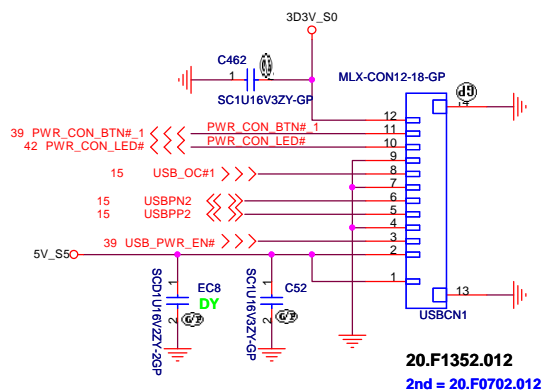
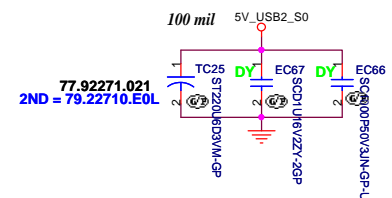
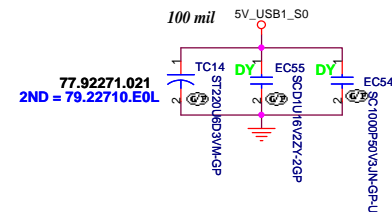
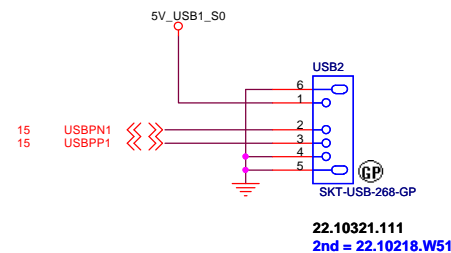
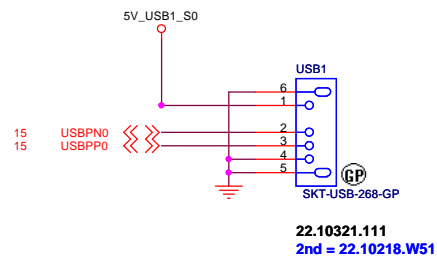
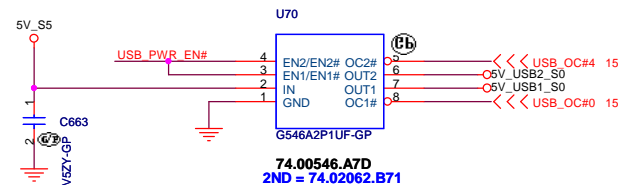
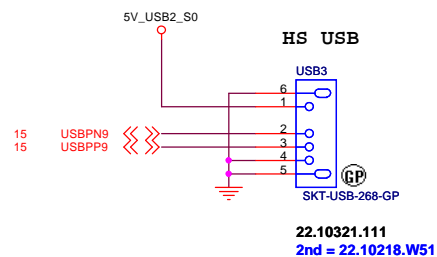
**JV70-CP**

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|  |                 |
|--|-----------------|
| <b>緯創資通</b><br><b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                 |
| Title<br><b>USB CONN</b>   |                 |
| Size   | Document Number |
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- 1

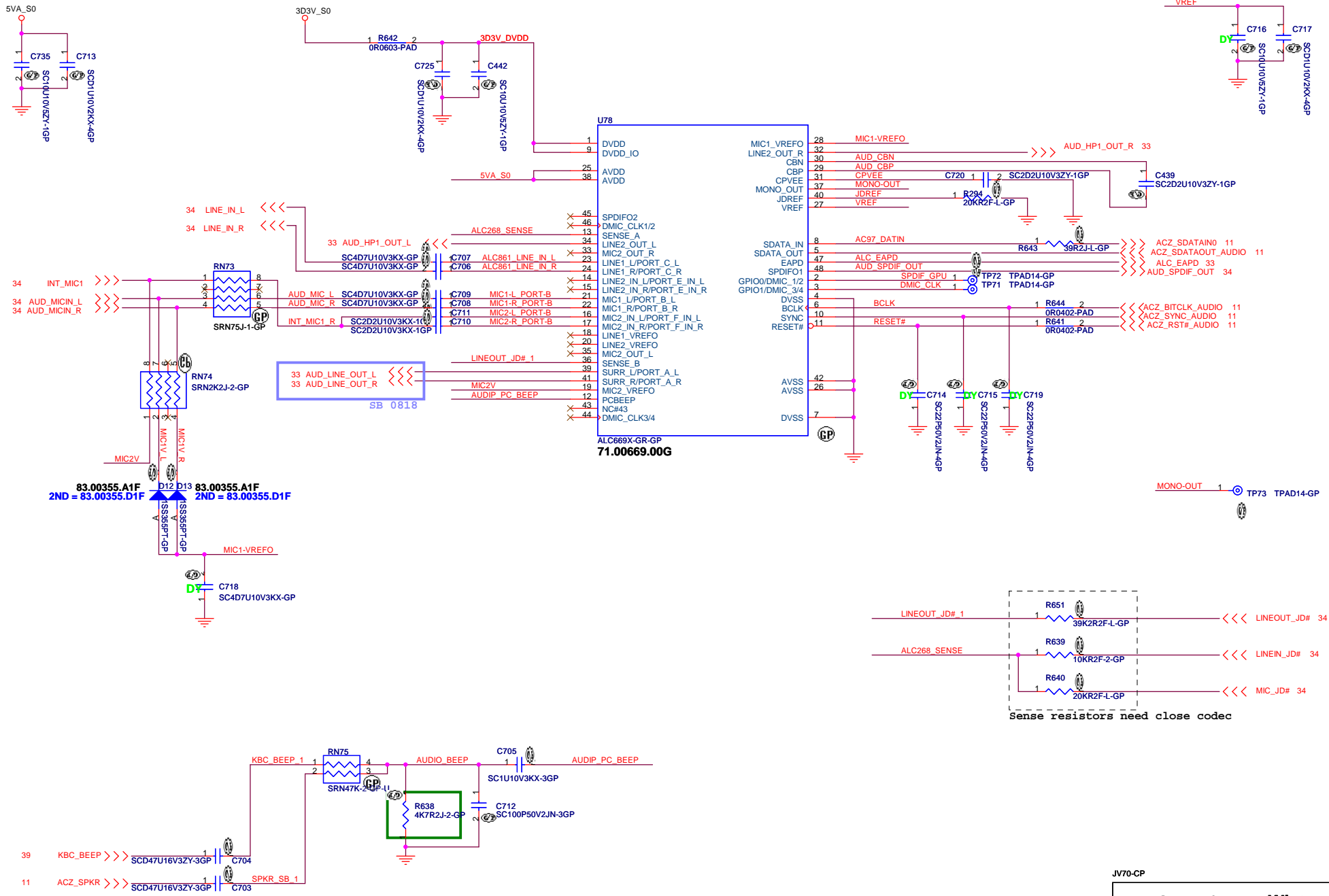
## C



## E

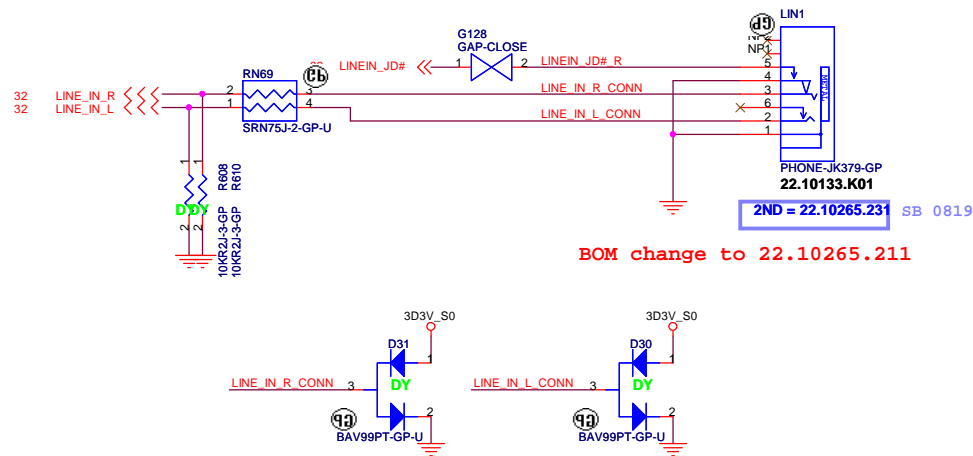


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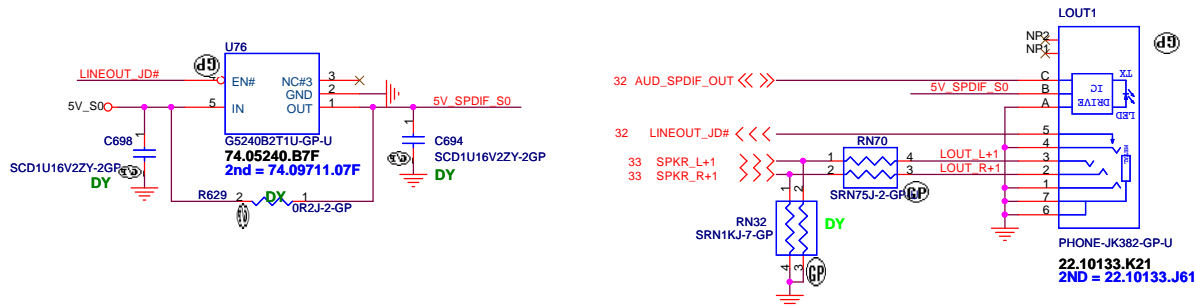




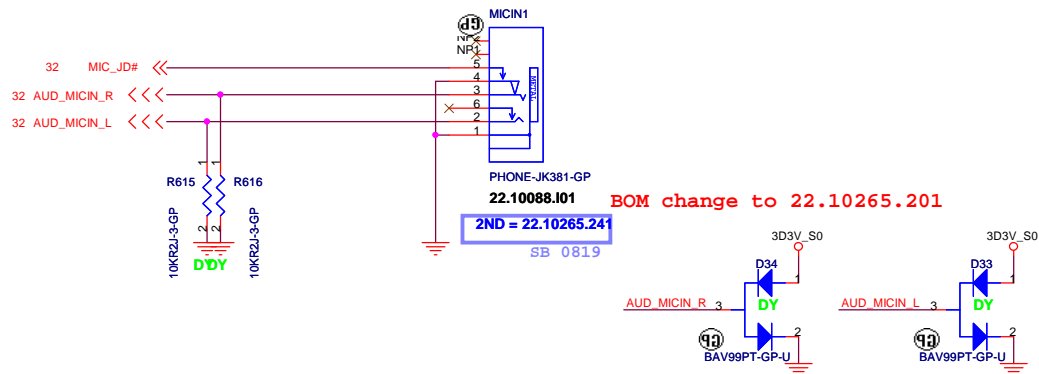
## LINE IN



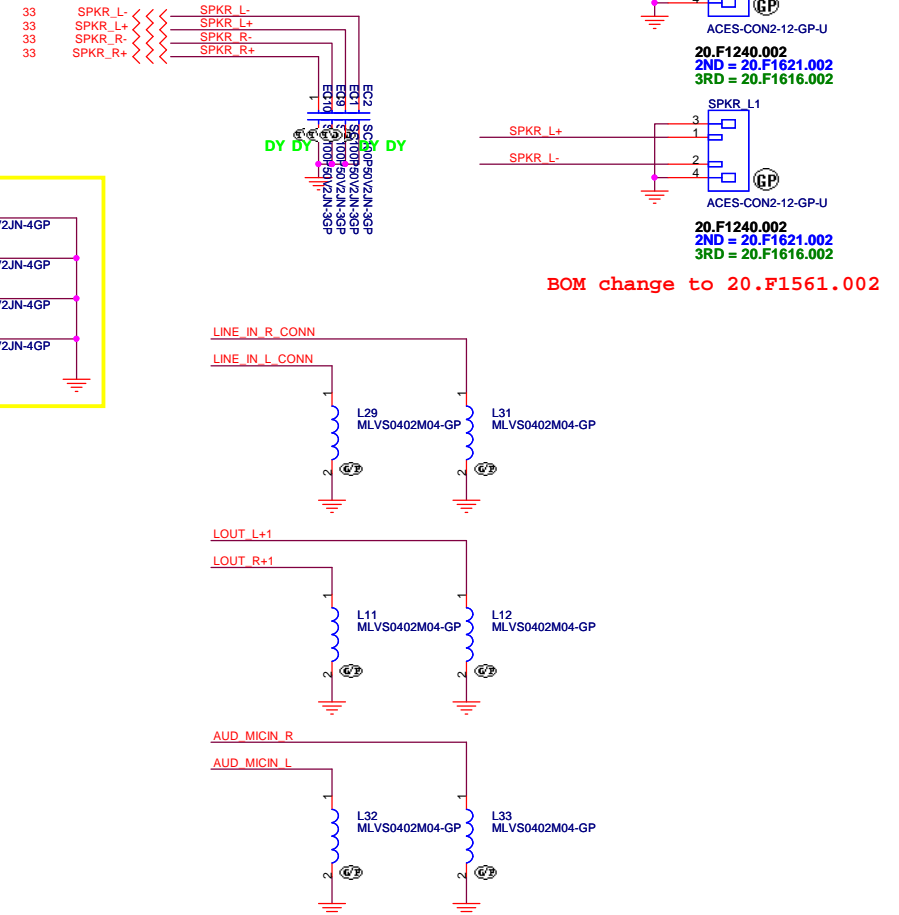
## LINE OUT



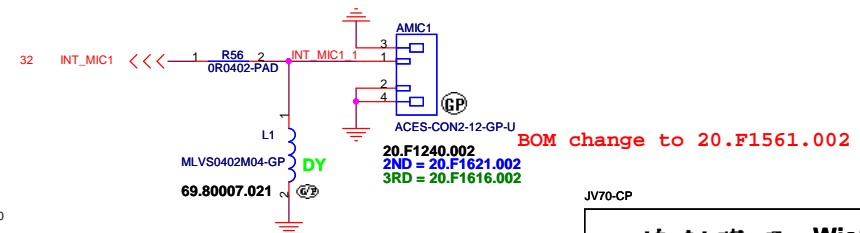
## MIC IN



## Internal Speaker



## Internal Mic

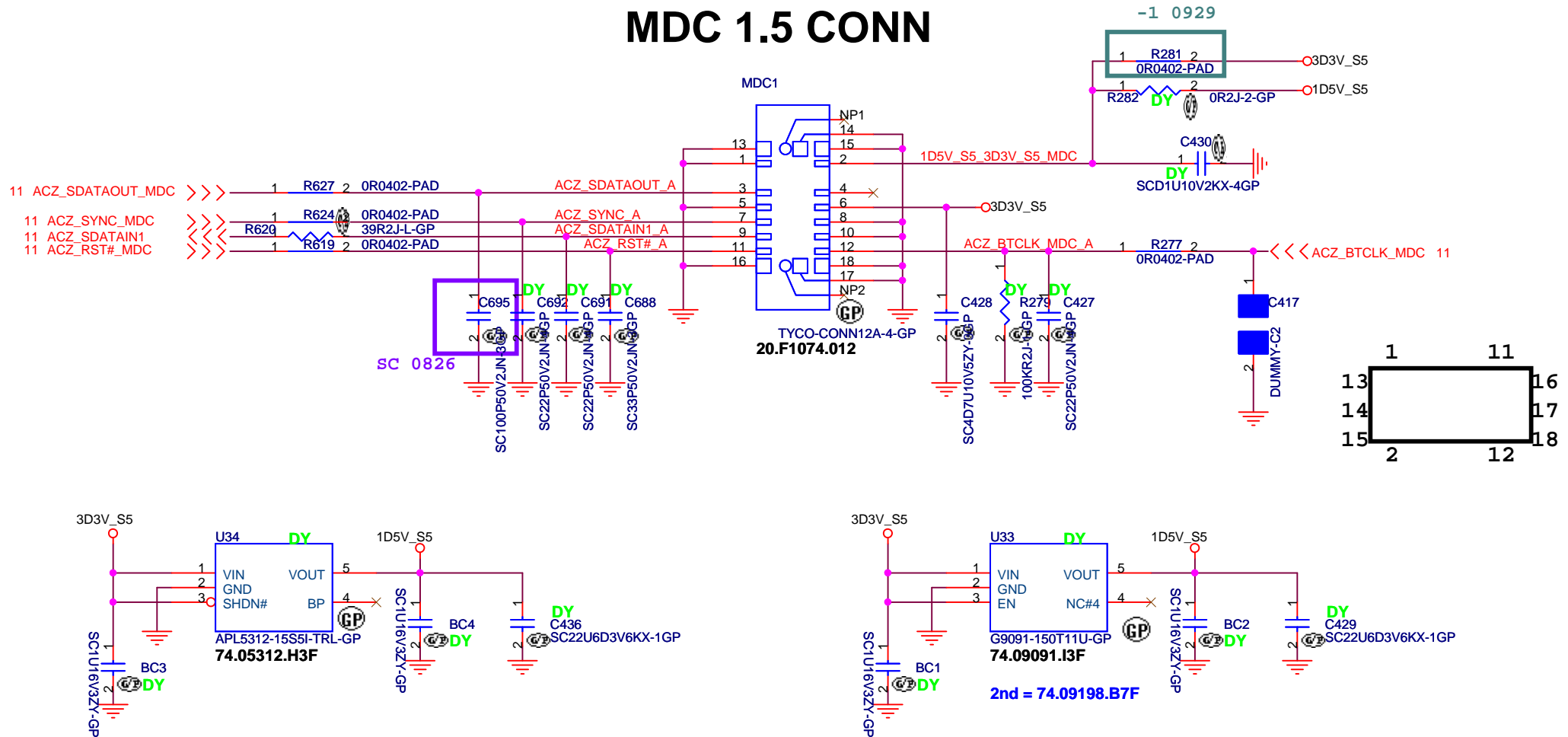


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| Title                            |                 |     |
|----------------------------------|-----------------|-----|
| AUDIO Jack                       |                 |     |
| Size                             | Document Number | Rev |
|                                  | JV70-CP         | -1  |
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# MDC 1.5 CONN



JV70-CP

緯創資通

**Wistron Corporation**

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Title

**MDC**

Size

Document Number

**JV70-CP**

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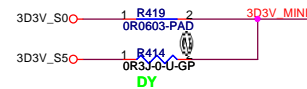
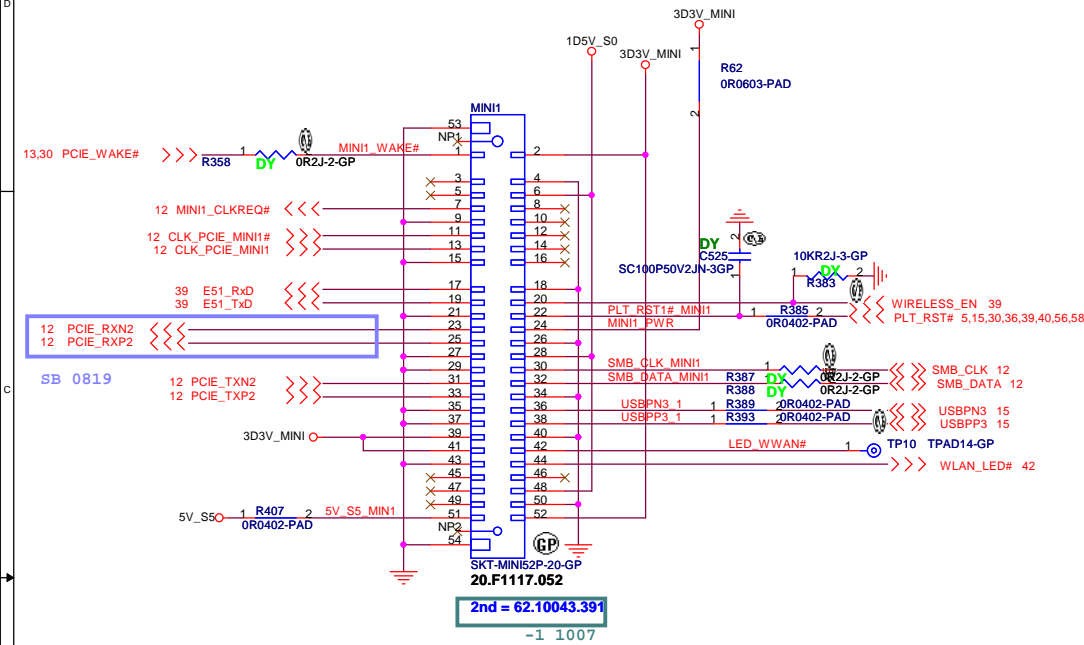




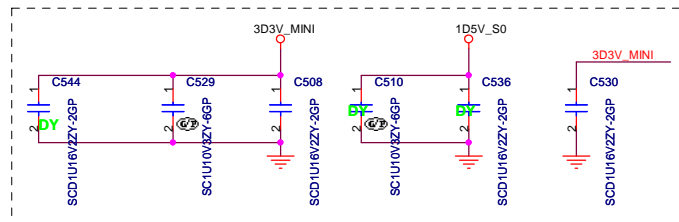
# Mini Card Connector(WLAN)

## Support debug-card

# Mini Card Connector



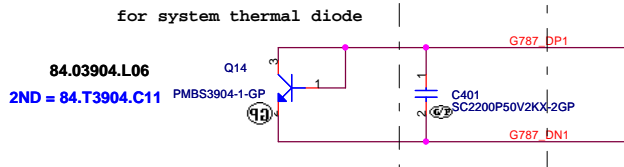
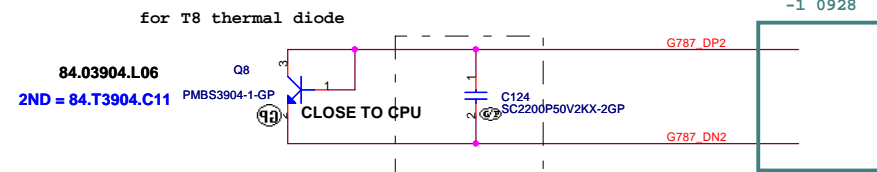
Place near MINI1



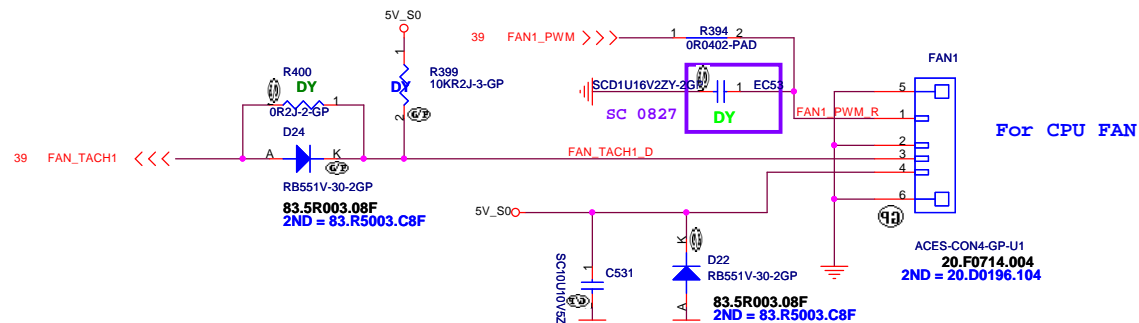
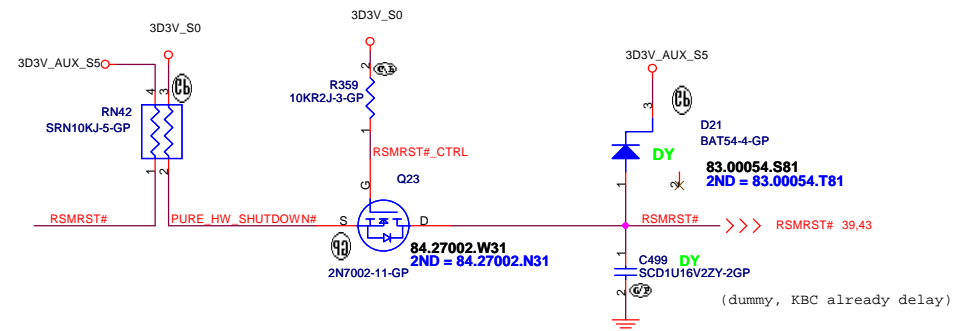
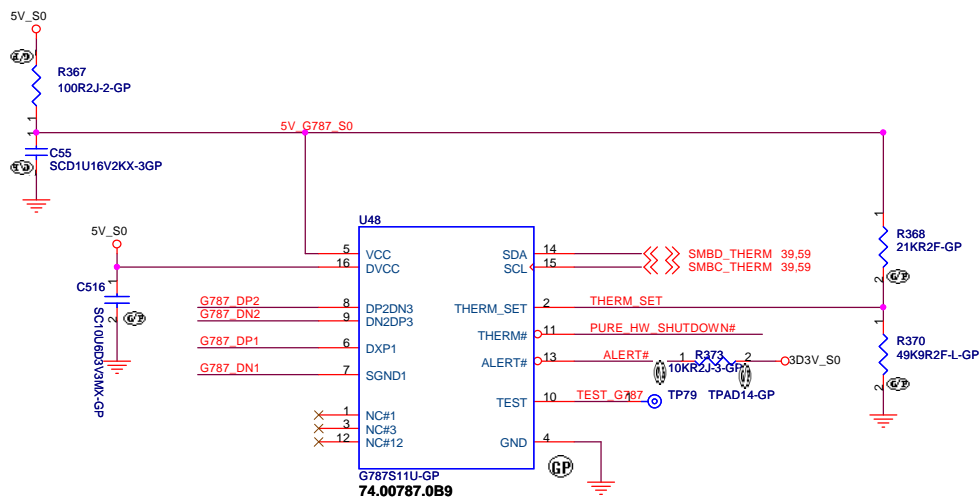
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|       |                            |       |           |
|-------|----------------------------|-------|-----------|
| Title |                            |       | MINI CARD |
| Size  | Document Number            | Rev   |           |
| A3    | JV70-CP                    | -1    |           |
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C124 & C401 CLOSE TO G787

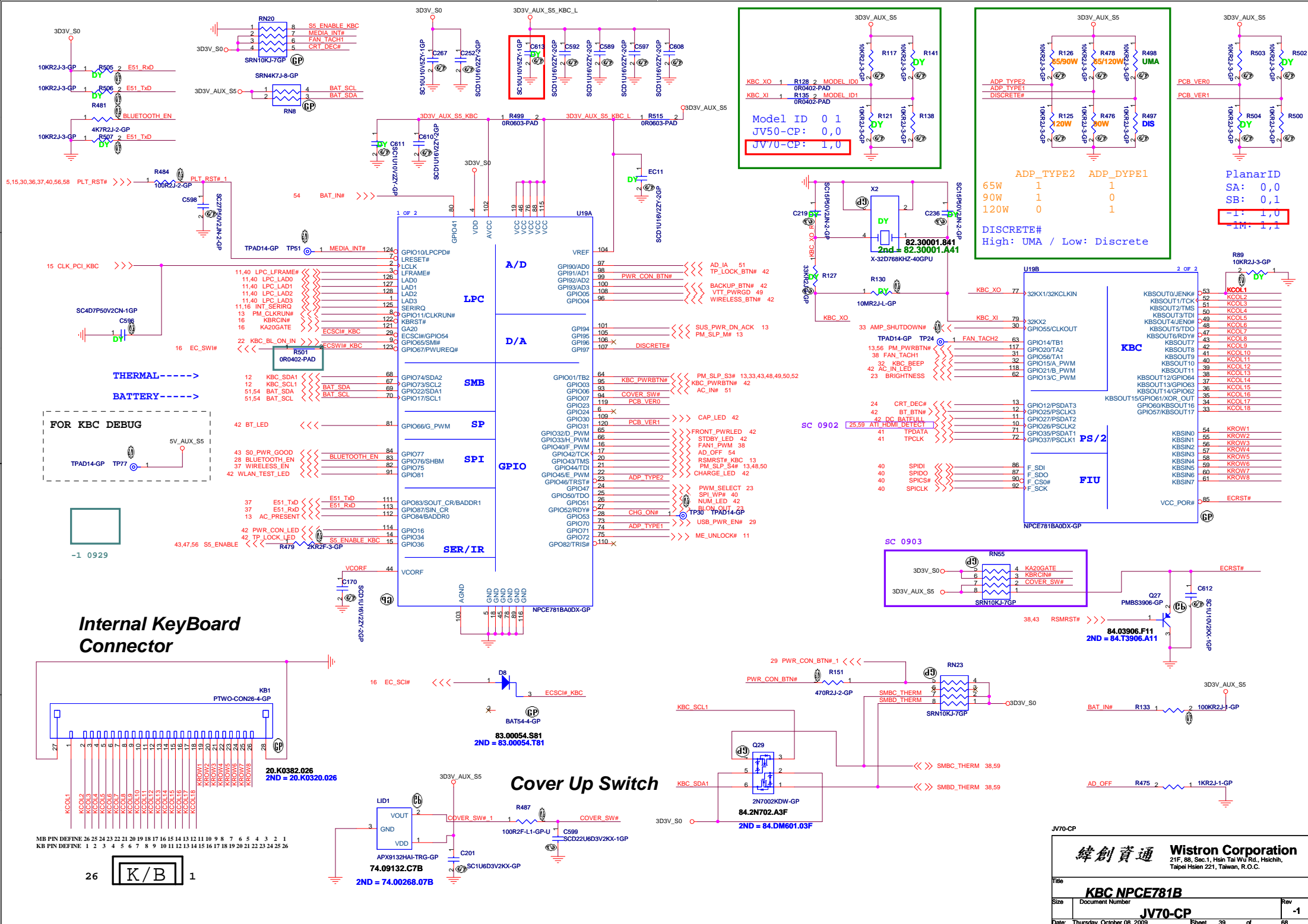


T8=90

$$\text{THERM\_SET} = [(T_{\text{set}} - 72) \times 0.02 + 0.34] \times \text{VCC}$$

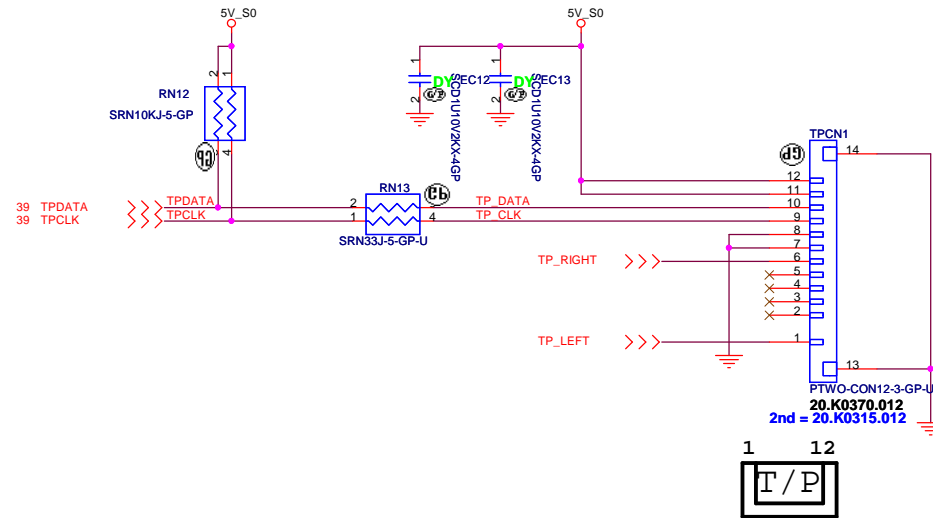
JV70-CP

|   |                 |                            |  |
|---|-----------------|----------------------------|--|
| <b>緯創資通</b>   |                 | <b>Wistron Corporation</b> |  |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                 |                            |  |
| <b>Thermal/Fan Connector</b>  |                 |                            |  |
| Size  | Document Number | Rev                        |  |
|   | JV70-CP         | -1                         |  |
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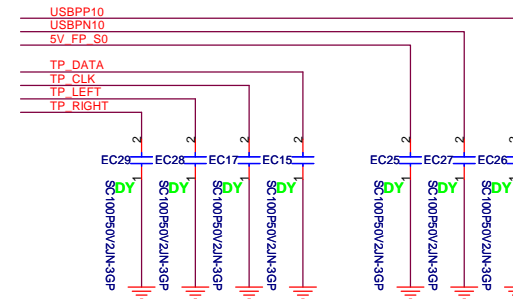
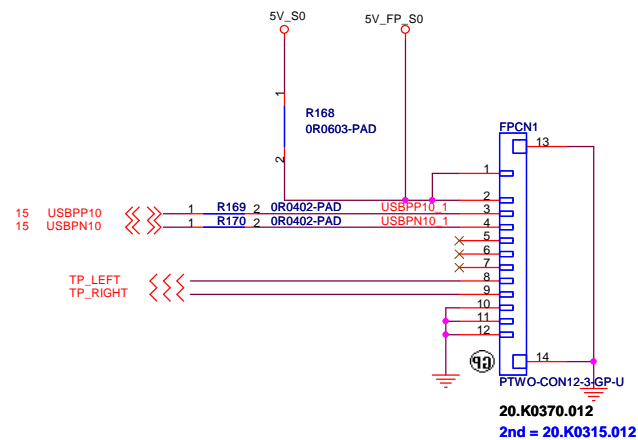




## TOUCH PAD



## Finger printer

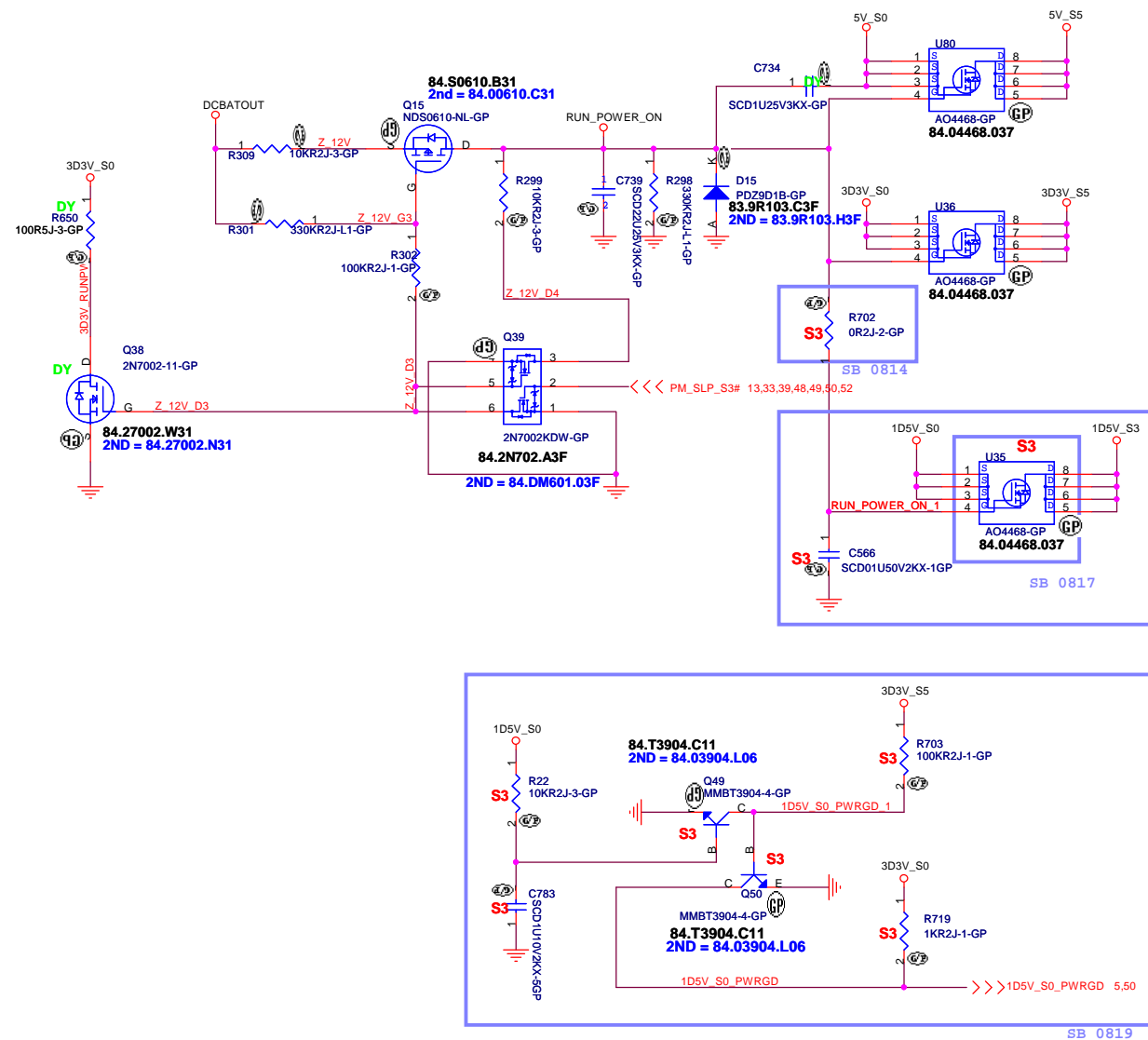


JV70-CP

|                         |                            |   |           |
|-------------------------|----------------------------|---|-----------|
| <b>緯創資通</b>             |                            | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |           |
| Title                   |                            |   |           |
| <b>Touch PAD and FP</b> |                            |   |           |
| Size                    | Document Number            |   | Rev       |
|                         | <b>JV70-CP</b>             |   | <b>-1</b> |
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## 3D3V\_AUX\_S5



緯創資通

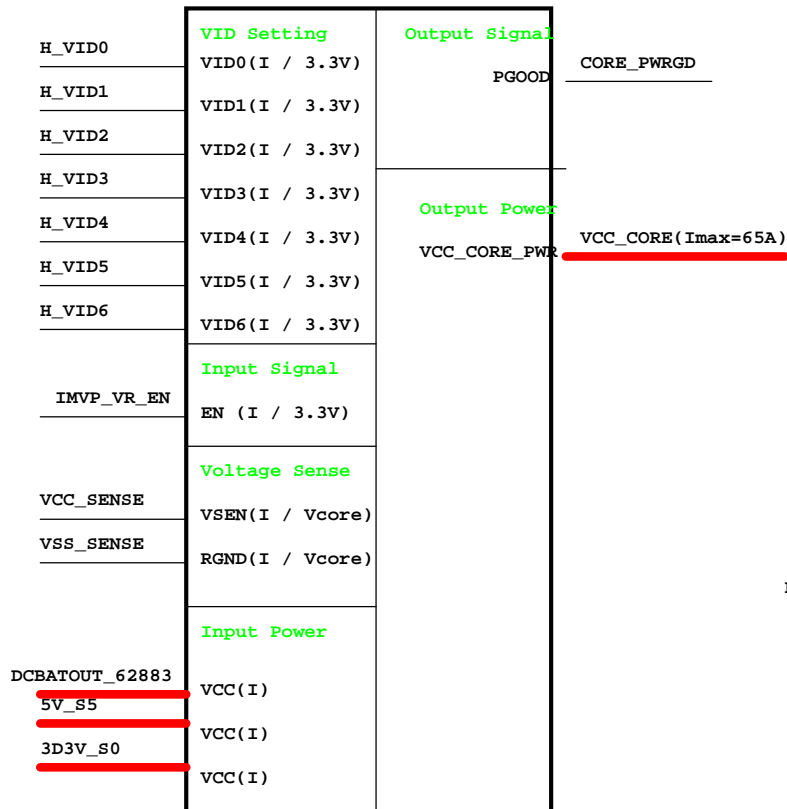
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

### ***RUN POWER and 3D3V AUX S5***

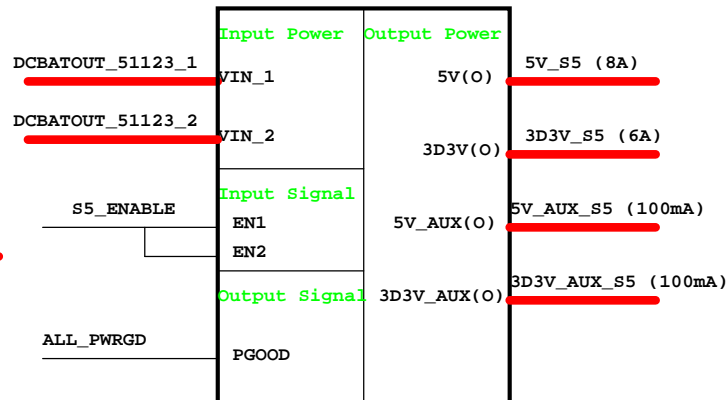
**JV70-CP**

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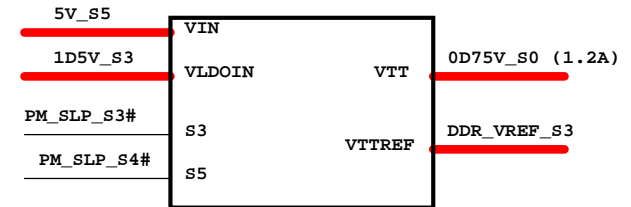
## ISL62883 VCC\_CORE



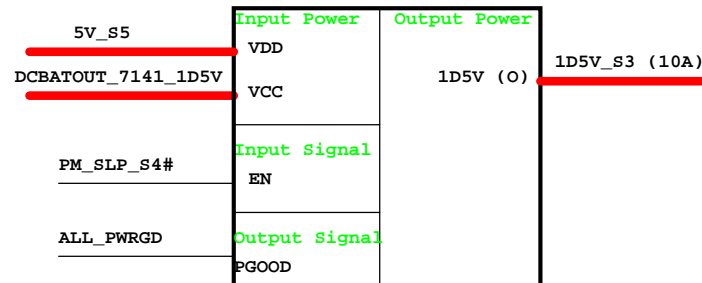
## TPS51123 5V/3D3V



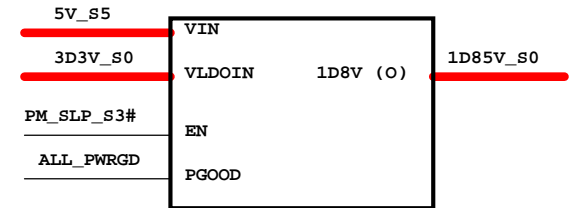
## G2997 0D75V\_S0



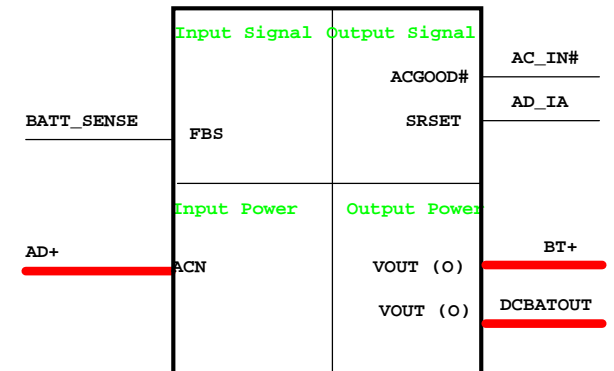
## TPS51117 1D5V



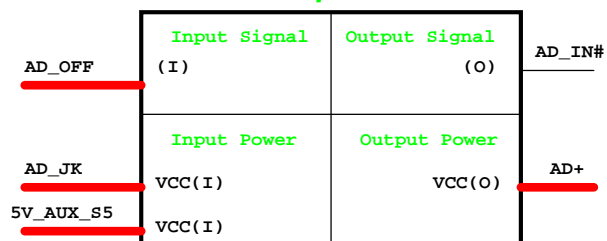
## RT9025 1D8V



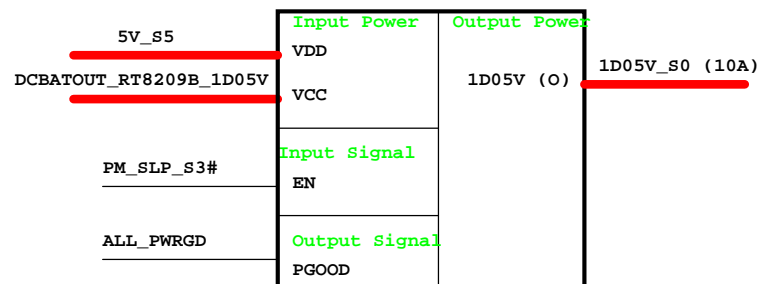
## Charger BQ24745



## Adapter



## TPS51117 1D05V

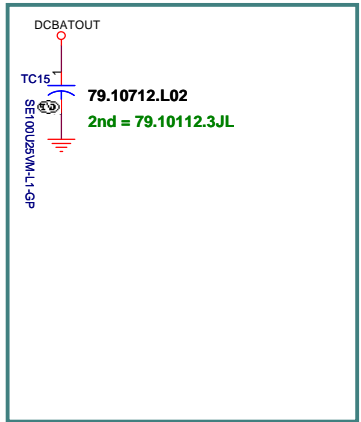


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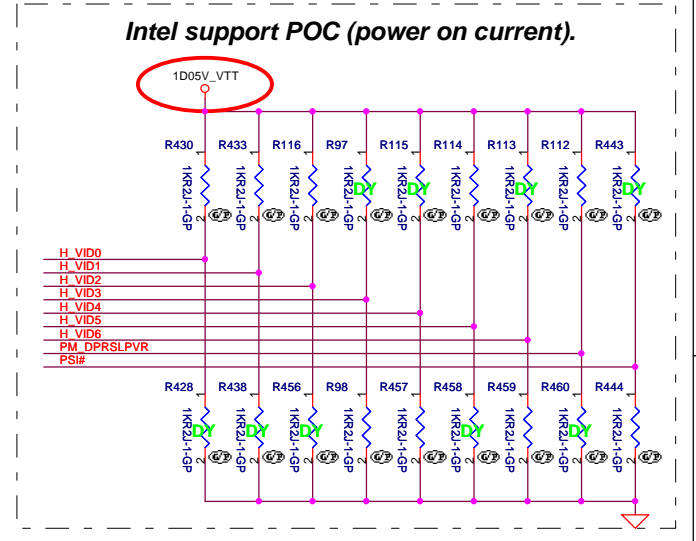
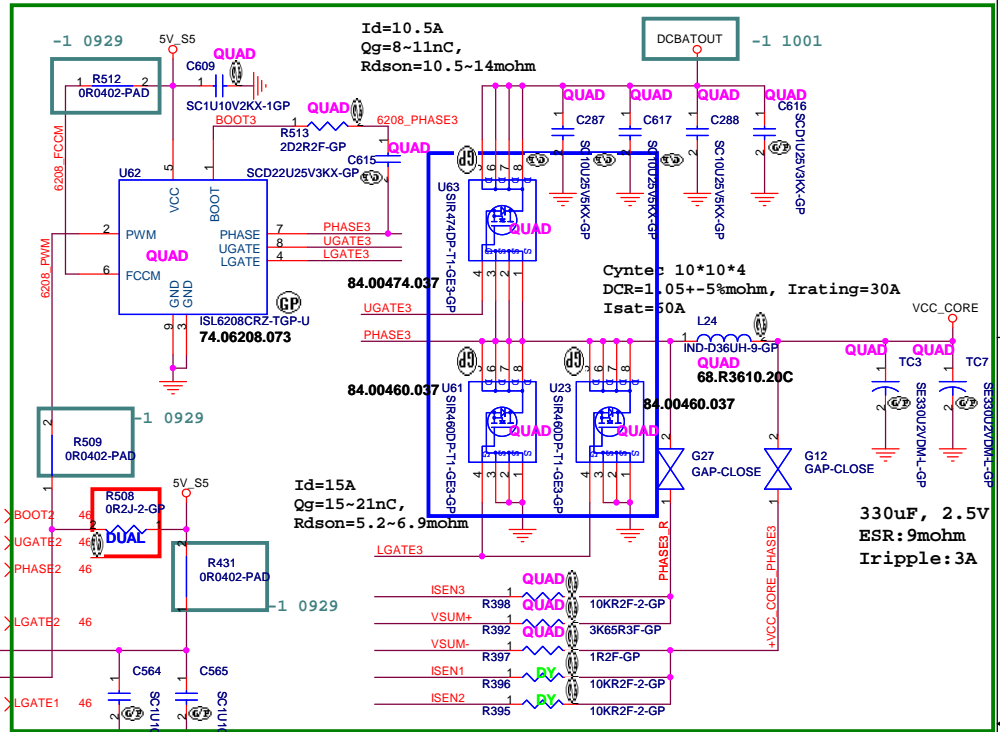
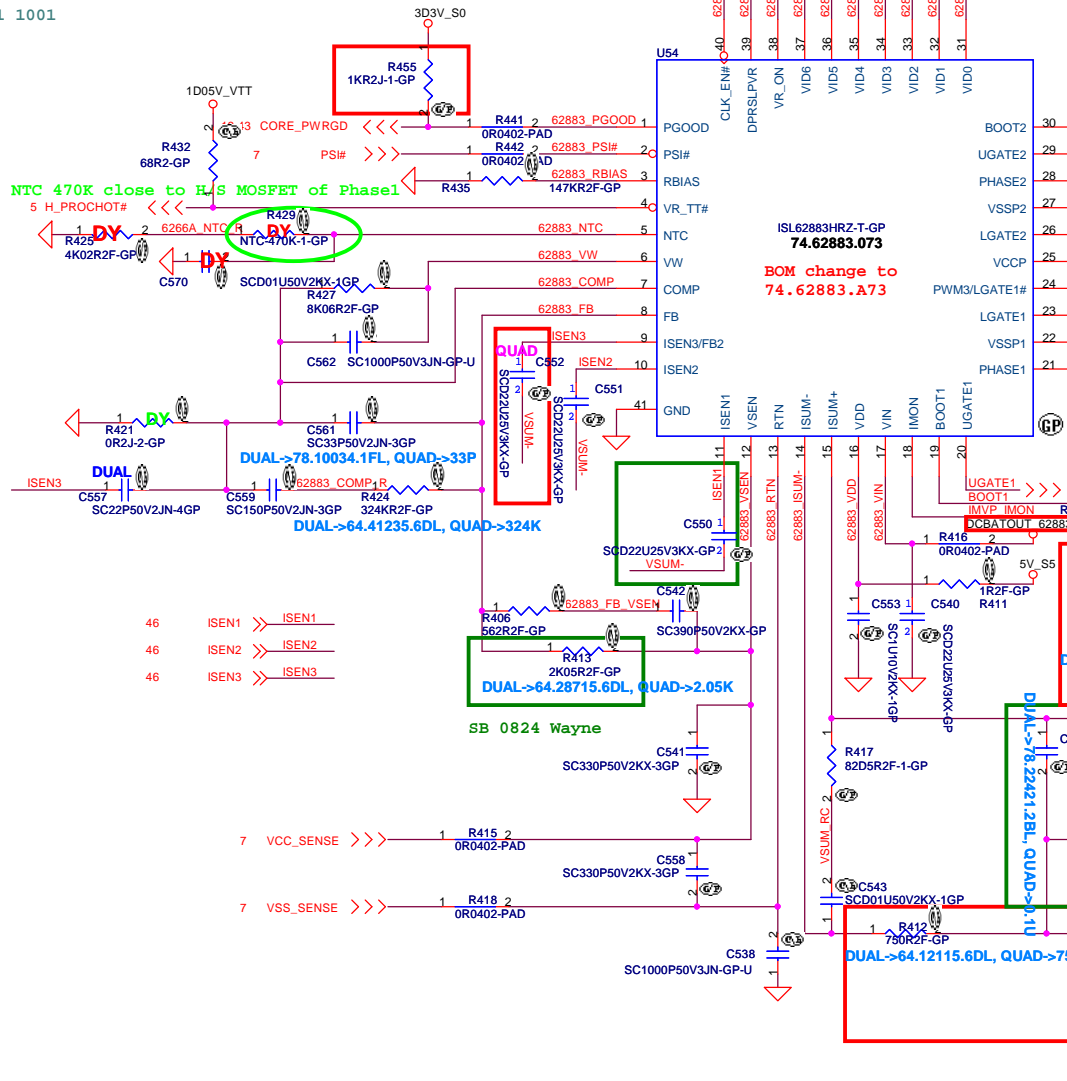
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

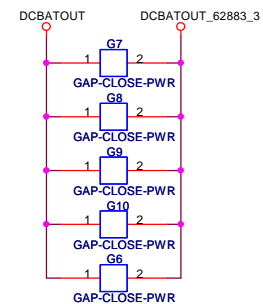
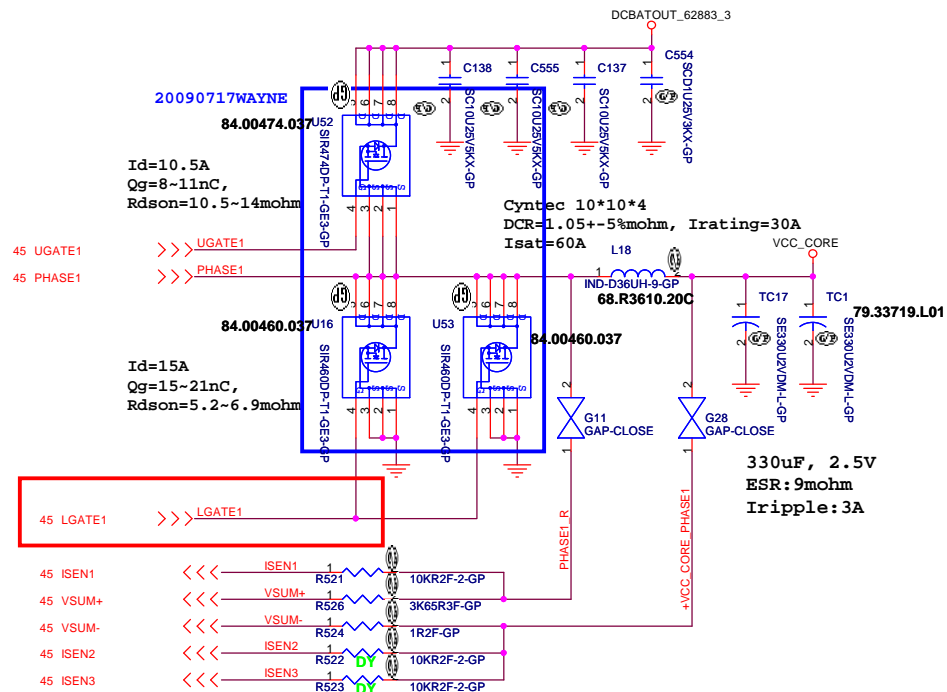
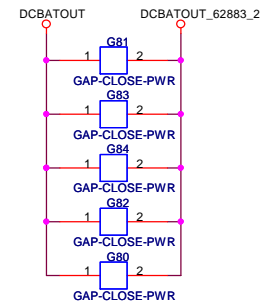
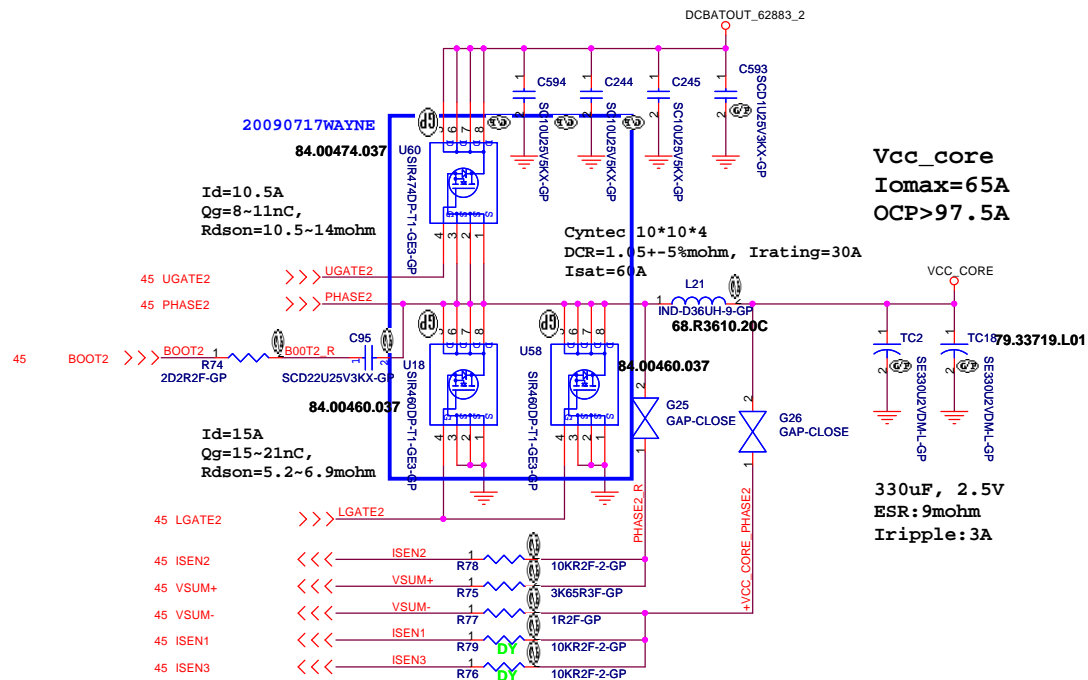
|   |                                   |                  |
|---|-----------------------------------|------------------|
| Title<br><b>Power Block Diagram</b>             |                                   |                  |
| Size  | Document Number<br><b>JV70-CP</b> | Rev<br><b>-1</b> |
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-1 1001

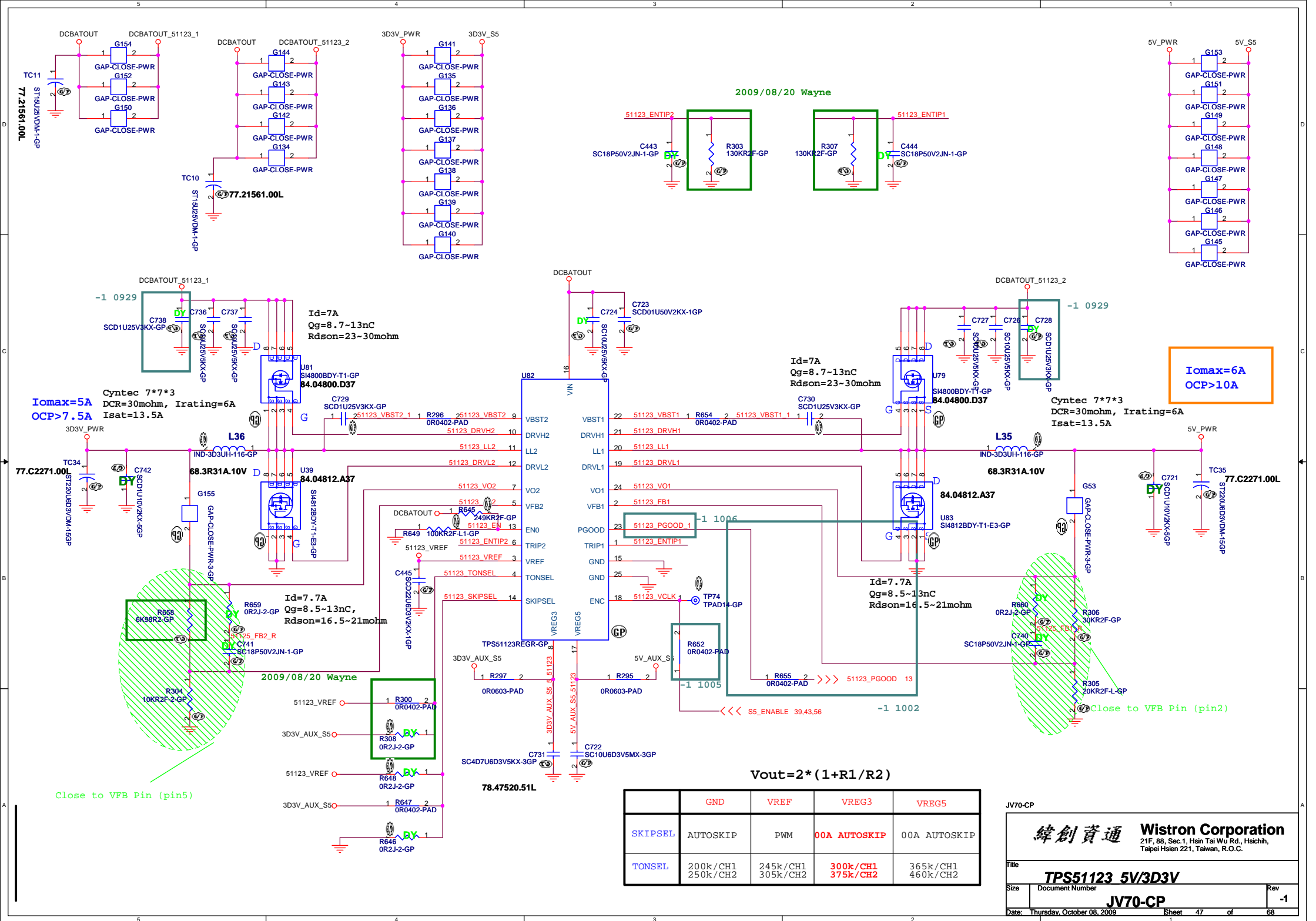




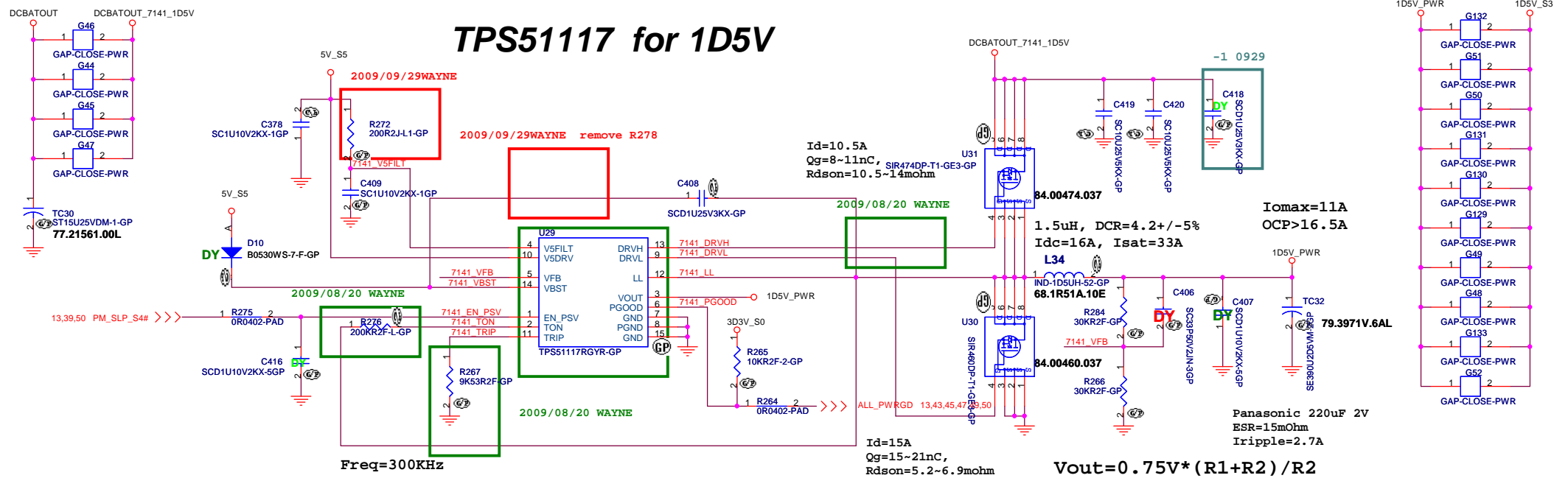
JV70-CP

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Taipei Hsien 221, Taiwan, R.O.C.

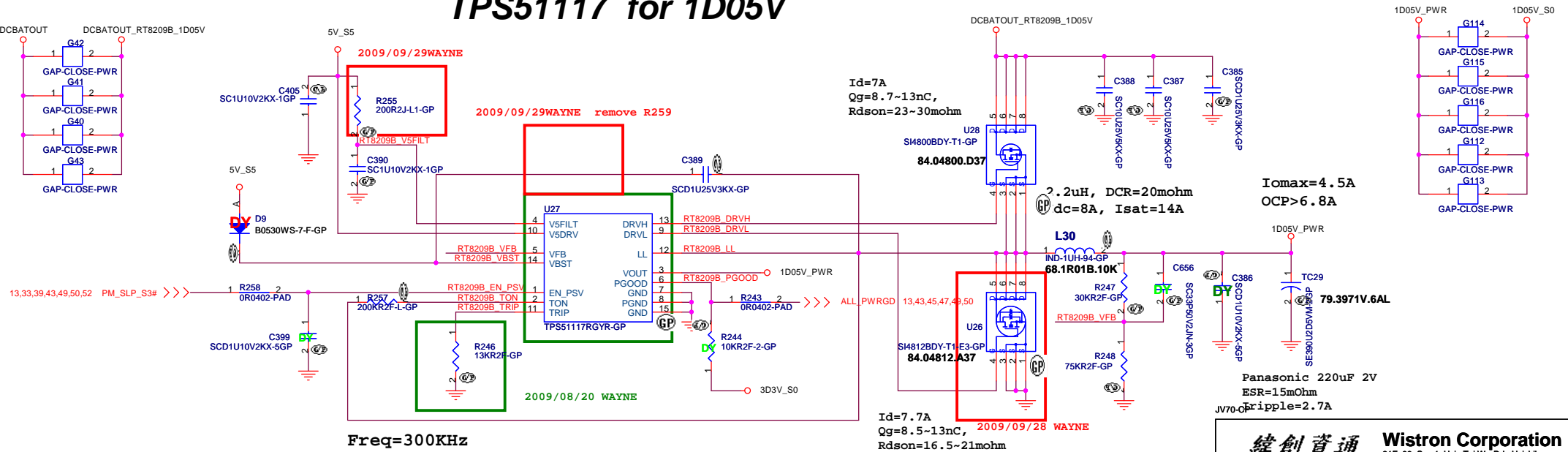
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| Title   |                            | ISL62883 CPU CORE ( 1/2 ) |          |
| Size    | Document Number            | Rev                       |          |
| JV70-CP |                            | -1                        |          |
| Date:   | Thursday, October 08, 2009 | Sheet                     | 46 of 68 |



## TPS51117 for 1D5V

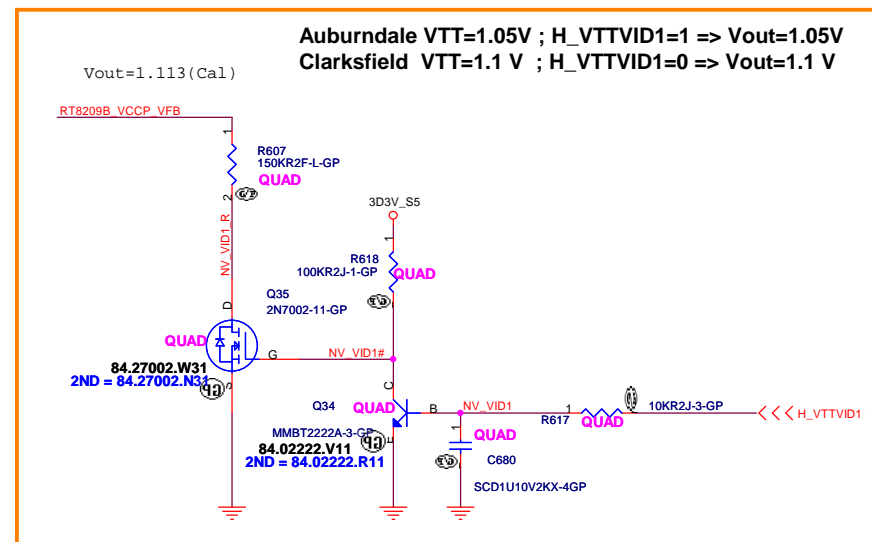
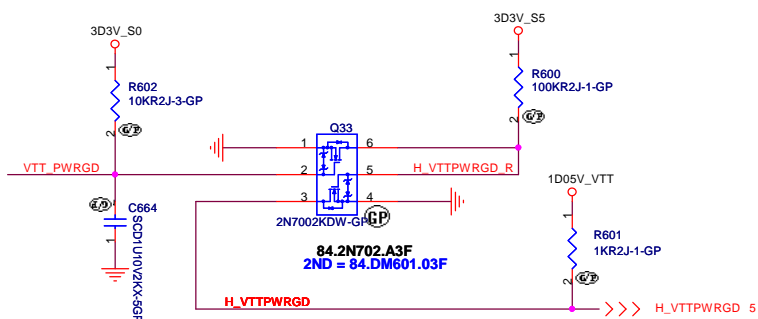


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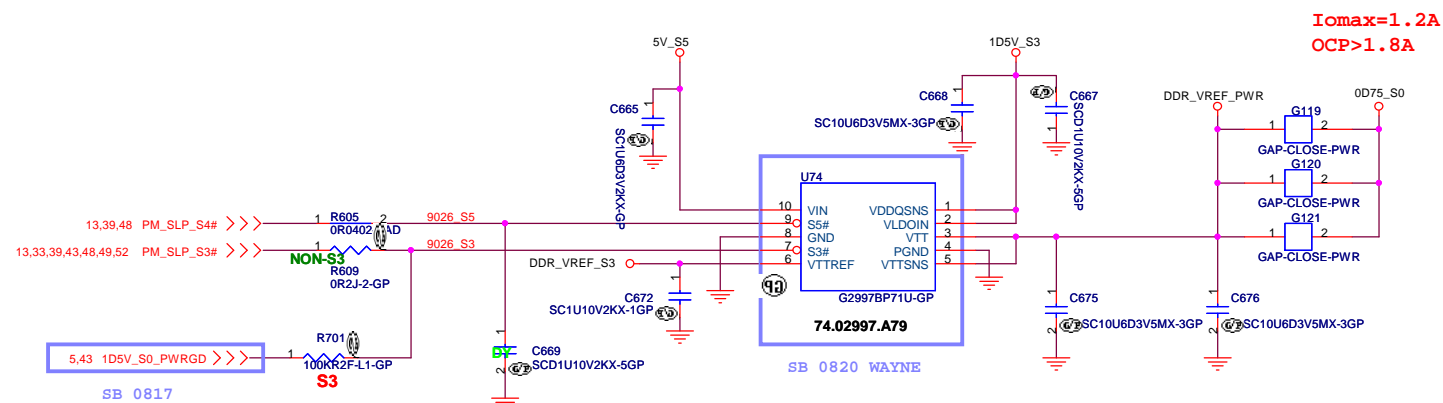


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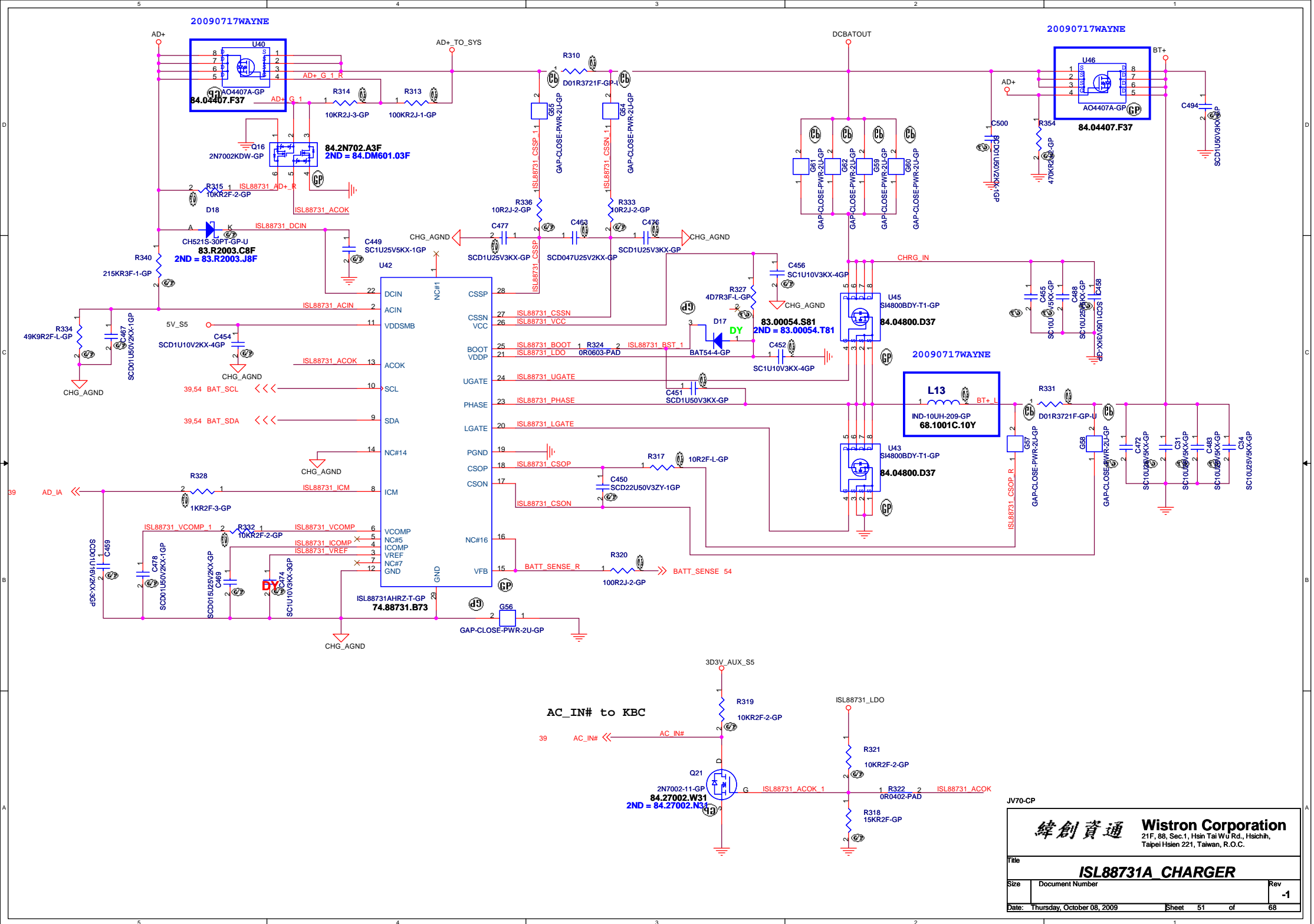
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| Size  | Document Number              |       | Rev      |
|       |                              |       | -1       |
| Date: | Thursday, October 08, 2009   | Sheet | 48 of 68 |



## G2997 for 0D75V\_S3



|                        |                            |             |     |
|------------------------|----------------------------|-------------|-----|
| Title                  |                            |             |     |
| RT9025 1D8V/G2997 0D75 |                            |             |     |
| Size                   | Document Number            |             | Rev |
|                        | JV70-CP                    |             | -1  |
| Date:                  | Thursday, October 08, 2009 | Sheet 50 of | 68  |

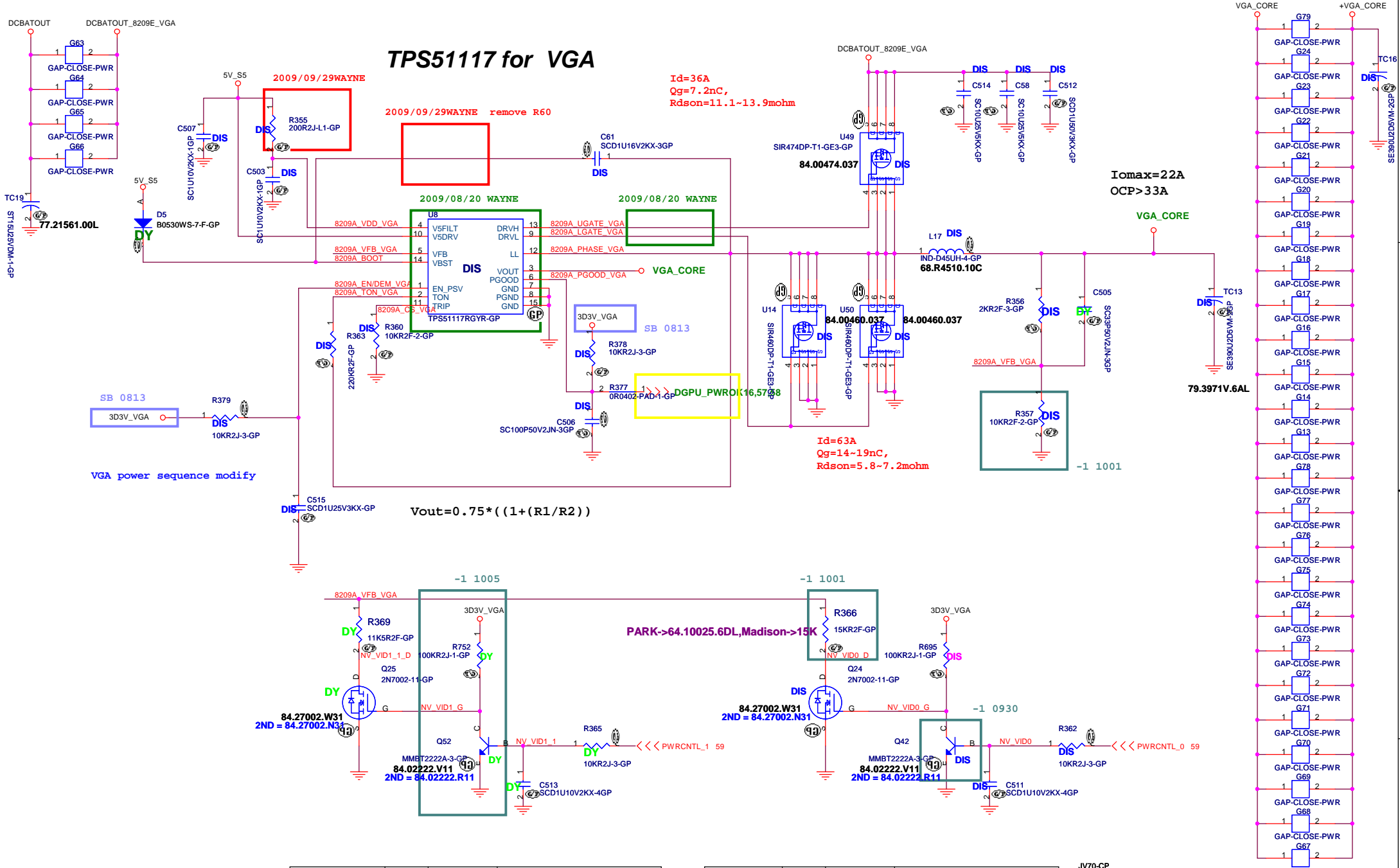








# TPS51117 for VGA



| Madison-Pro | I/O | Inter Pull Low | GPIO TABLE  |         |
|-------------|-----|----------------|-------------|---------|
| PWRCNTL_0   | O   | YES            | GPU VOLTAGE | L: 1.0V |
|             |     |                | GPU VOLTAGE | H: 0.9V |

| Park-XT   | I/O | Inter Pull Low | GPIO TABLE  |          |
|-----------|-----|----------------|-------------|----------|
| PWRCNTL_0 | O   | YES            | GPU VOLTAGE | L: 1.05V |
|           |     |                | GPU VOLTAGE | H: 0.9V  |

JV70-CP

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Title

TPS51117 VGA CORE

Size A3

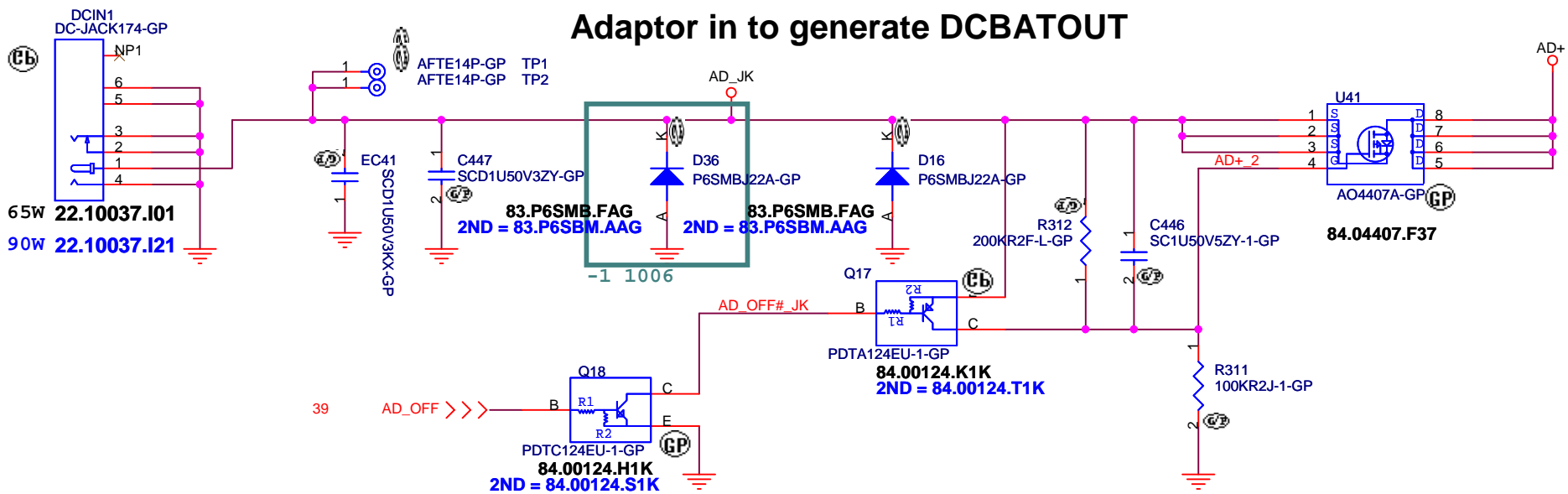
Document Number

Rev

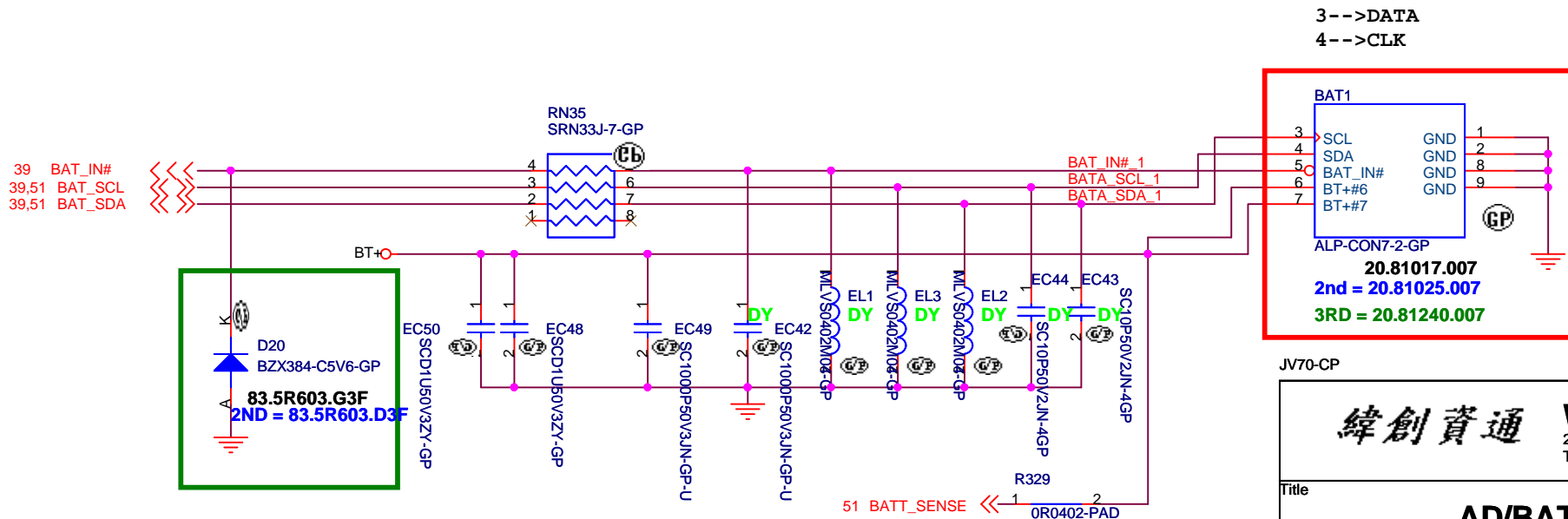
Thursday, October 08, 2009

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## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR



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Title

**AD/BATT CONN**

Size

Document Number

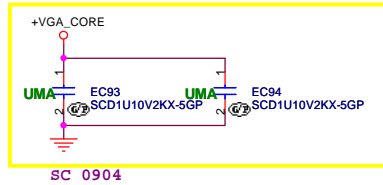
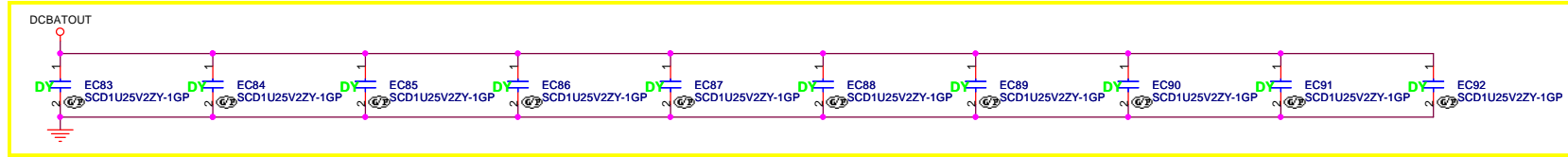
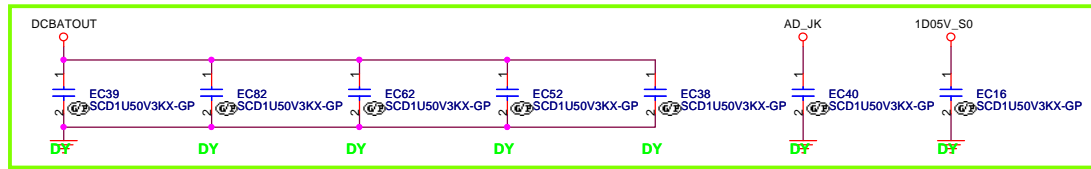
**JV70-CP**

Rev

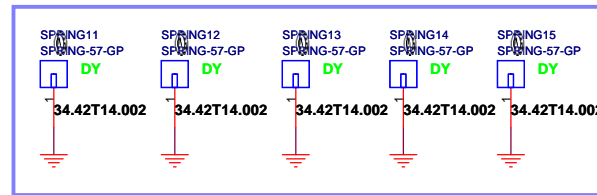
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Date: Thursday, October 08, 2009

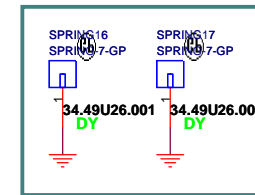
Sheet 54 of 68



TOP



TOP

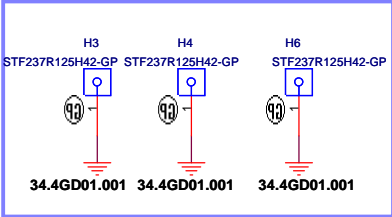


SB 0819

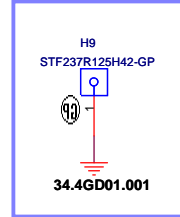
-1 0930

H1~H10 ALL IN TOP SIDE

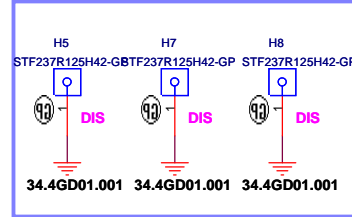
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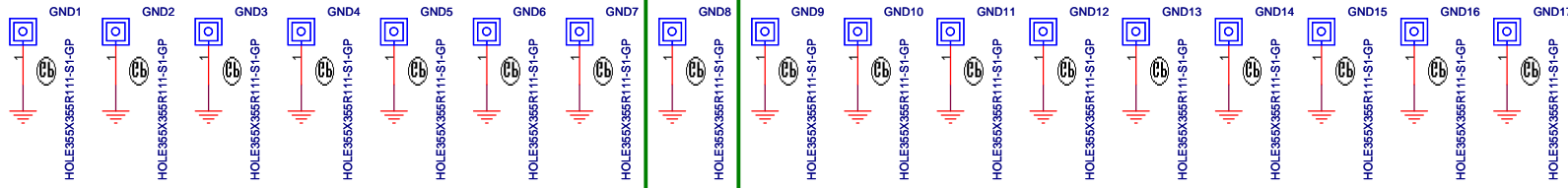
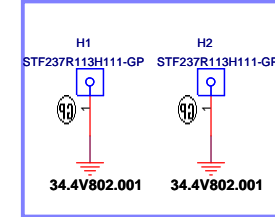
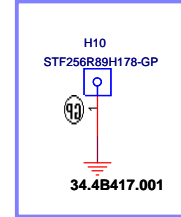
PCH



VGA



MDC



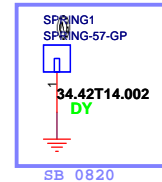
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BOT

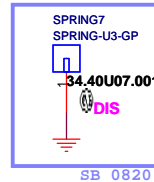
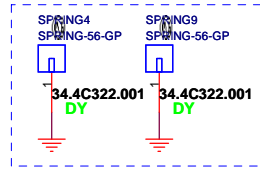
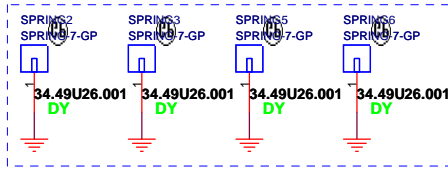
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BOT

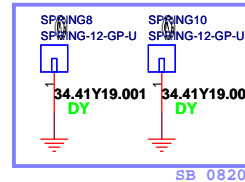
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SB 0820



SB 0820

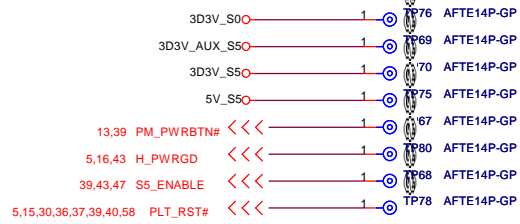


SB 0820

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|                                 |                 |   |       |
|---------------------------------|-----------------|---|-------|
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| <b>EMI/Spring/Boss</b>          |                 |   |       |
| Title                           | Document Number | Rev   |       |
| <b>JV70-CP</b>                  |                 | <b>-1</b>   |       |
| Date: Tuesday, October 13, 2009 |                 | Sheet 55  | of 68 |

## Check test point



Test Point放在Dimm Door打開可量測處

JV70-CP

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Title

AFTE TP

Size

Document Number

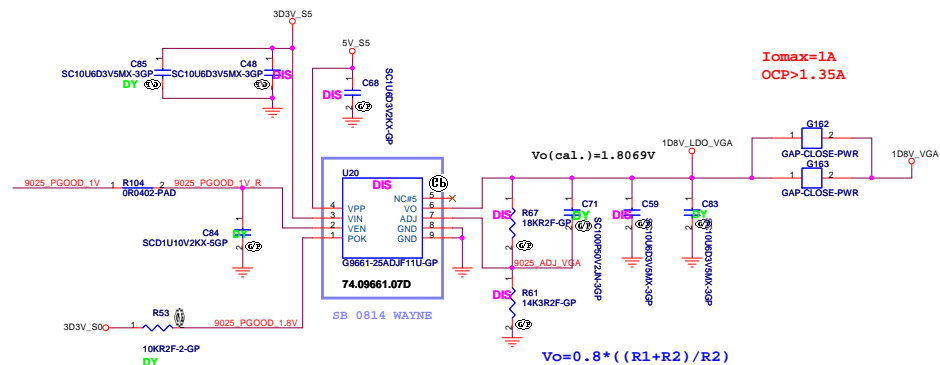
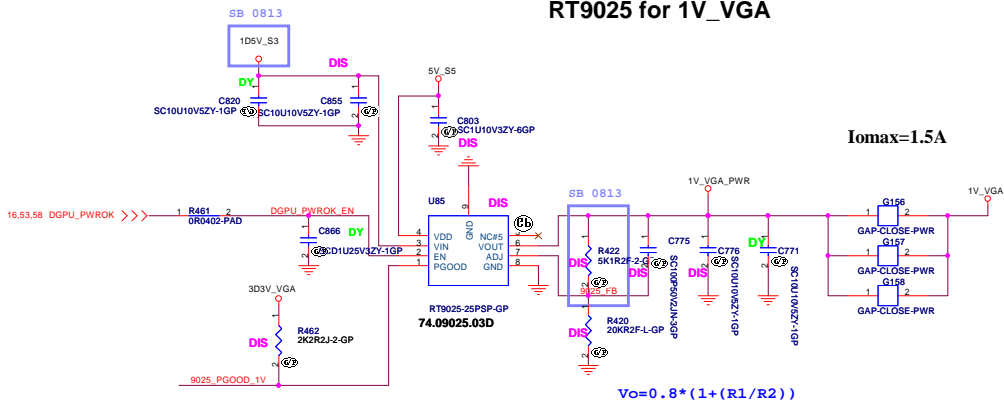
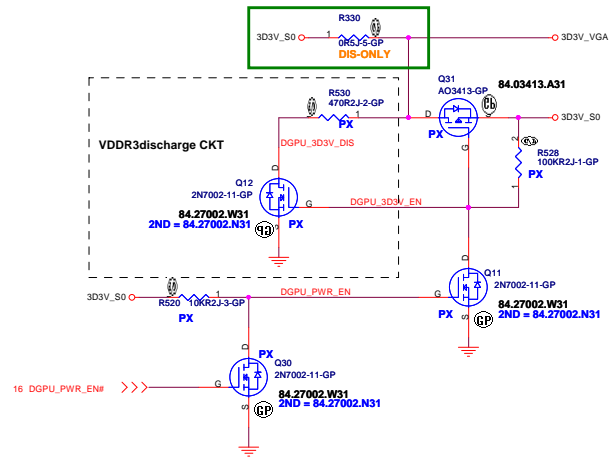
JV70-CP

Rev

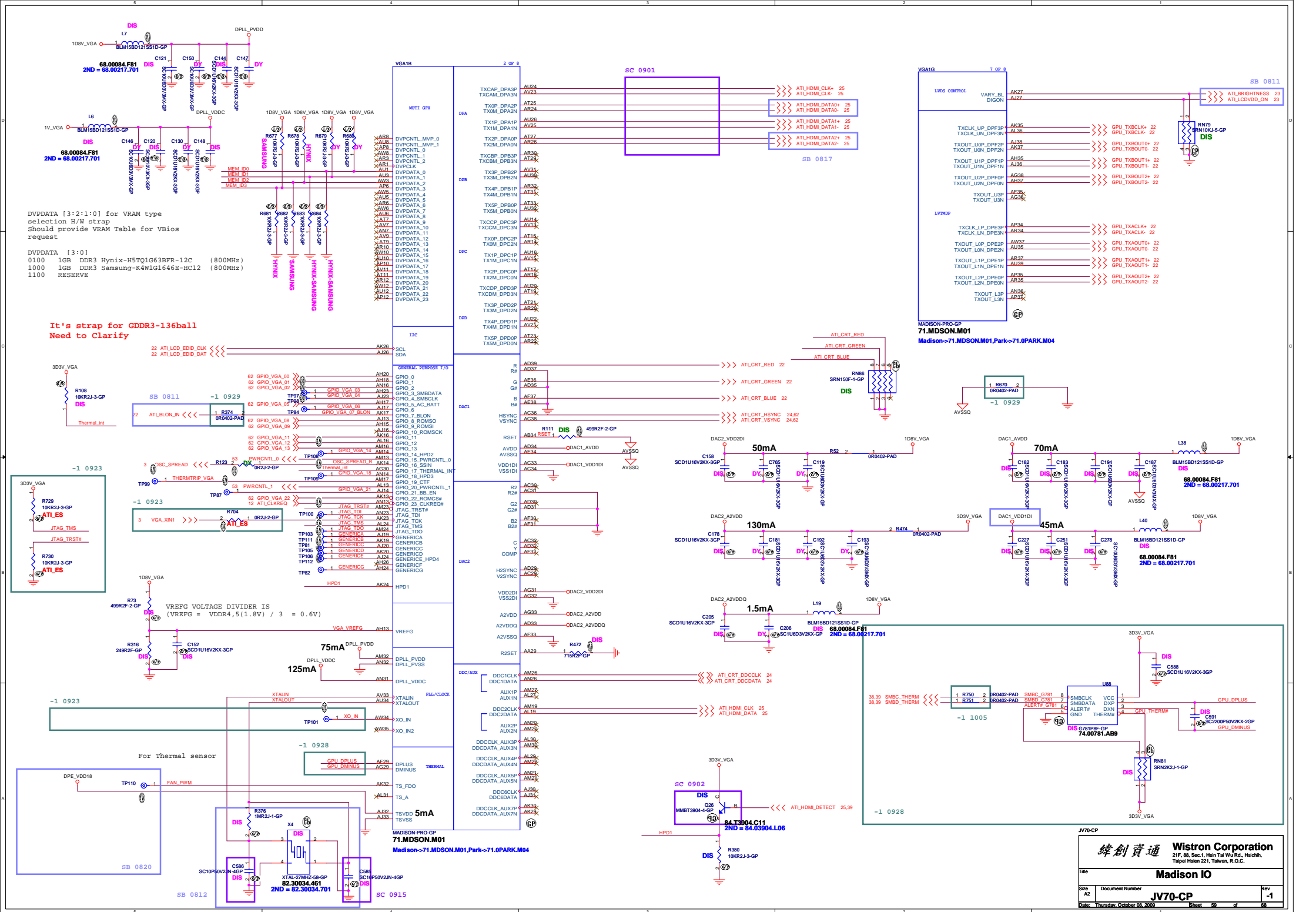
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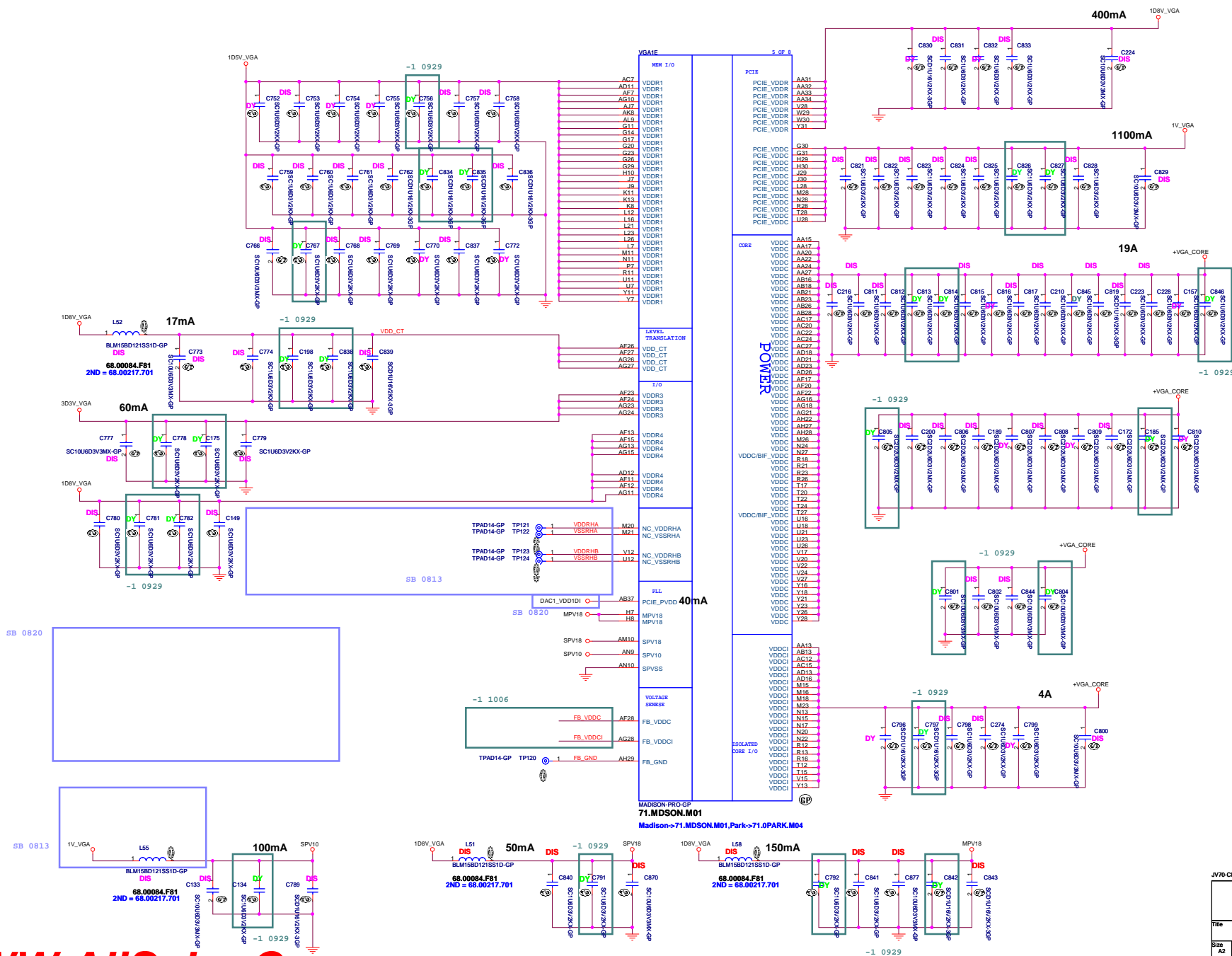
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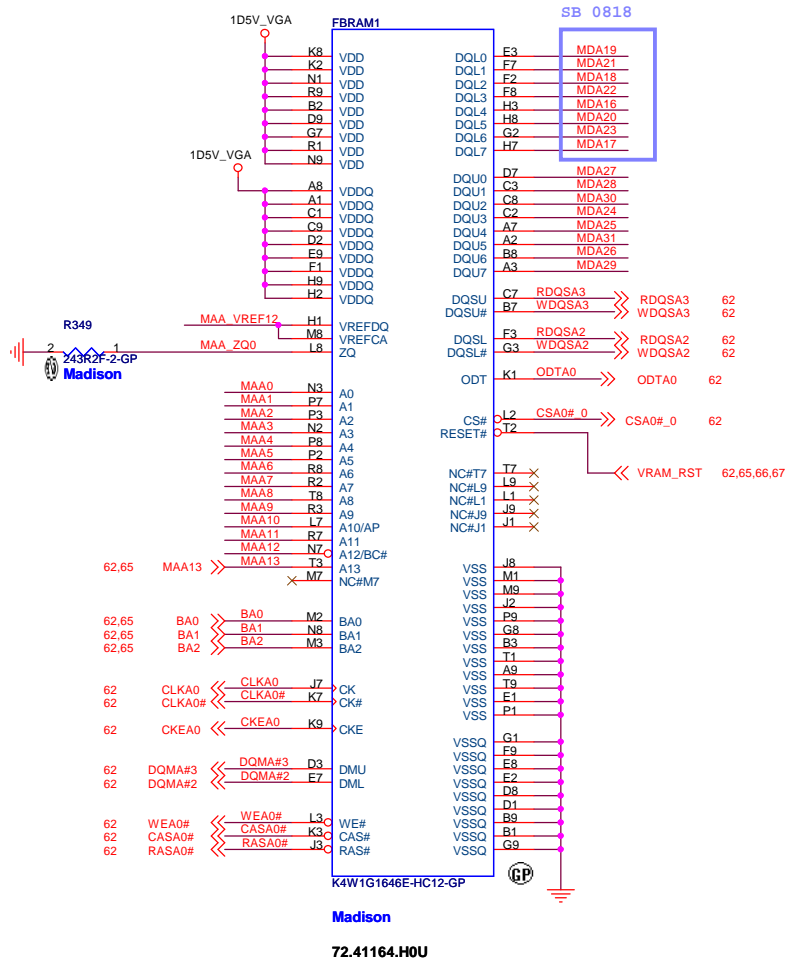




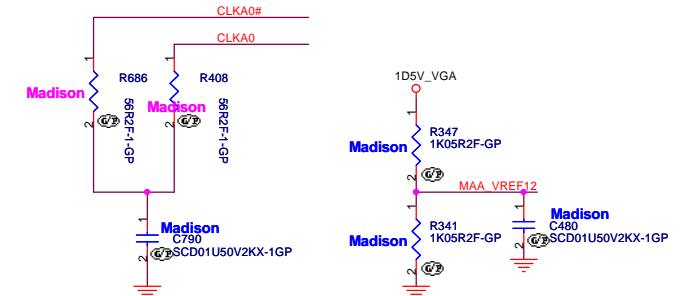
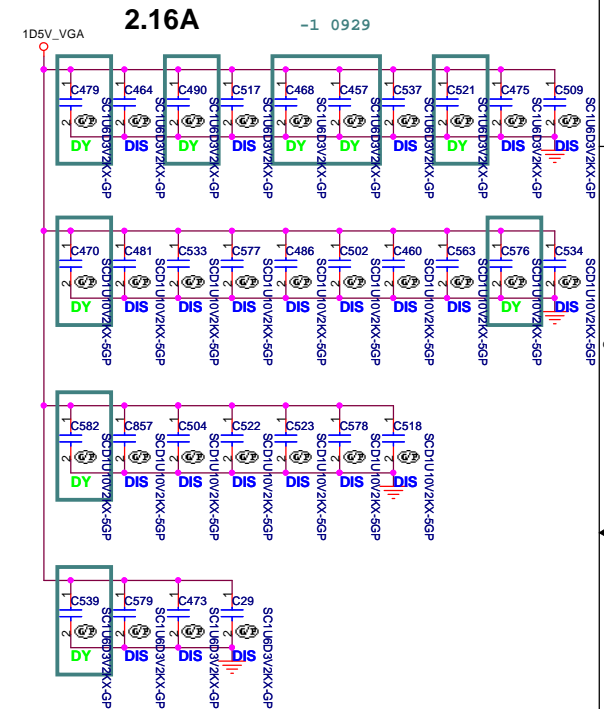
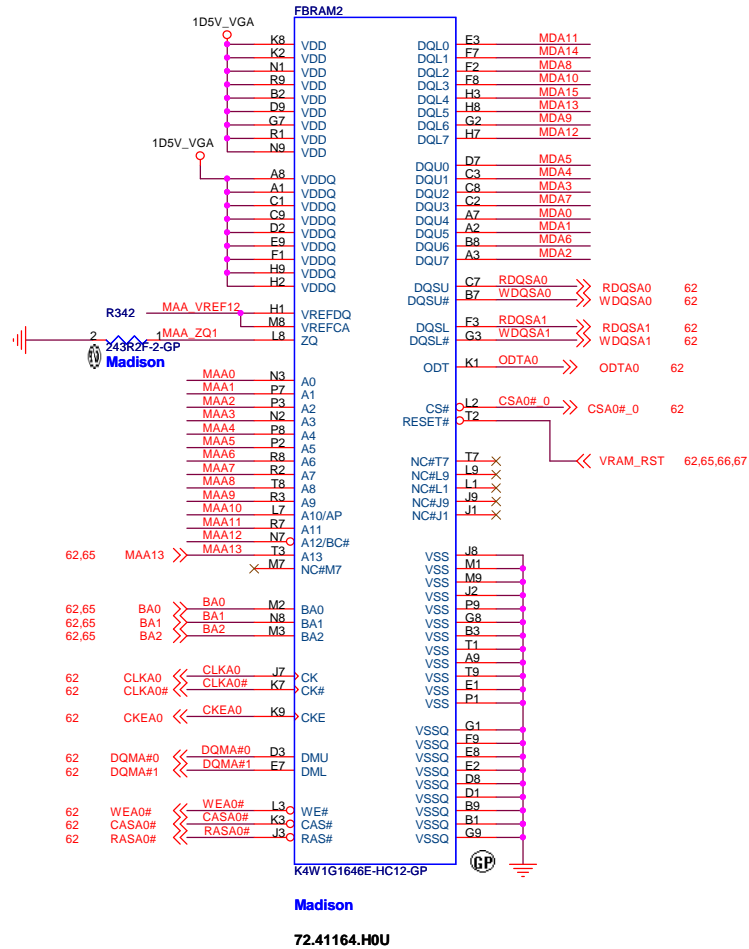
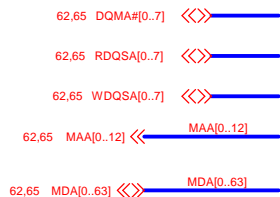




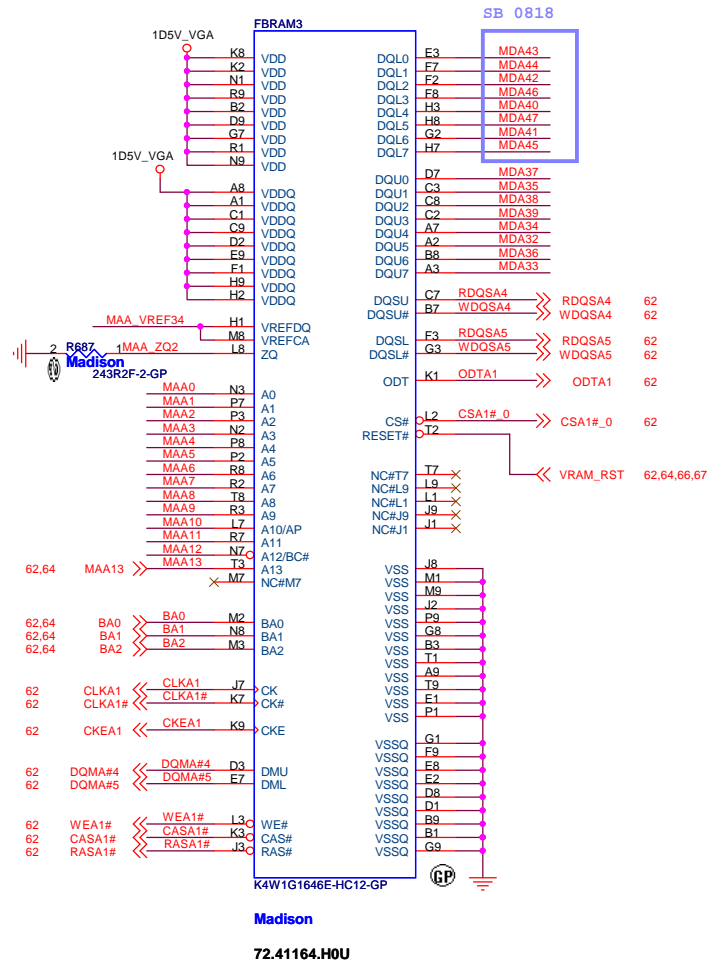
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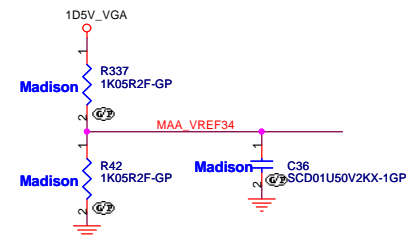
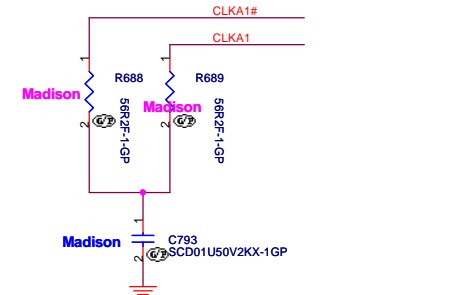
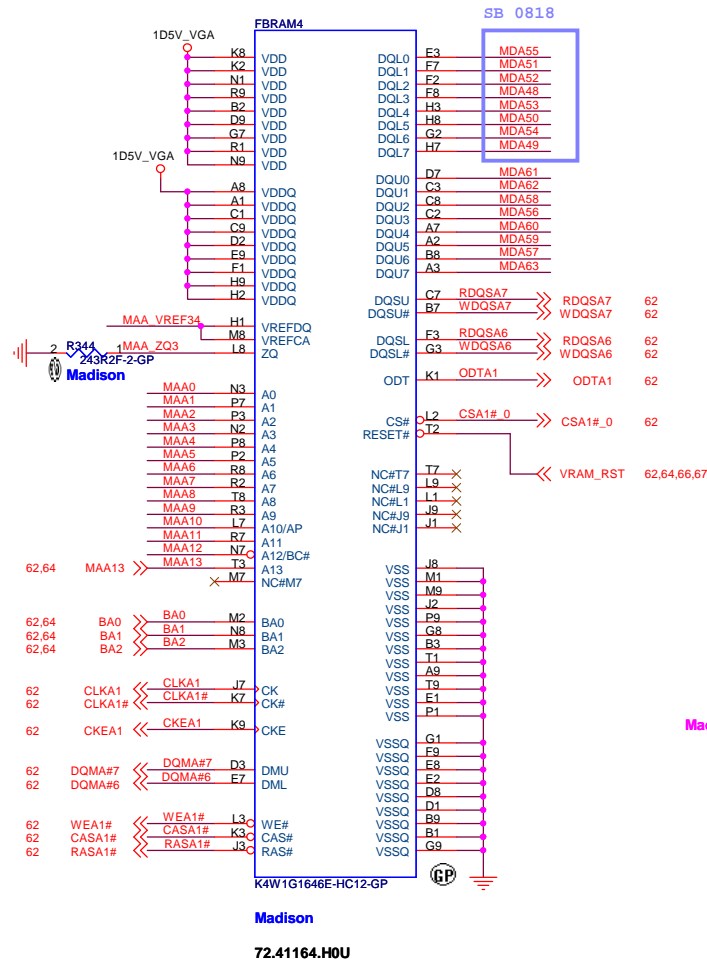
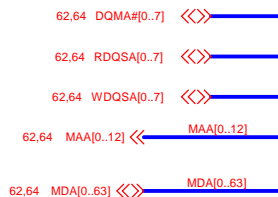
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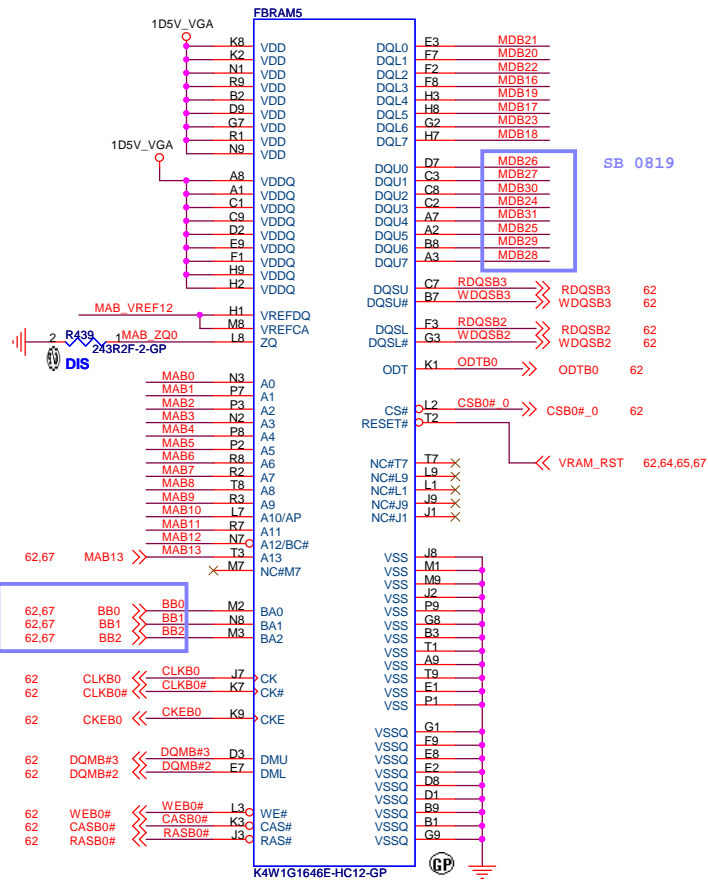
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# DDR3



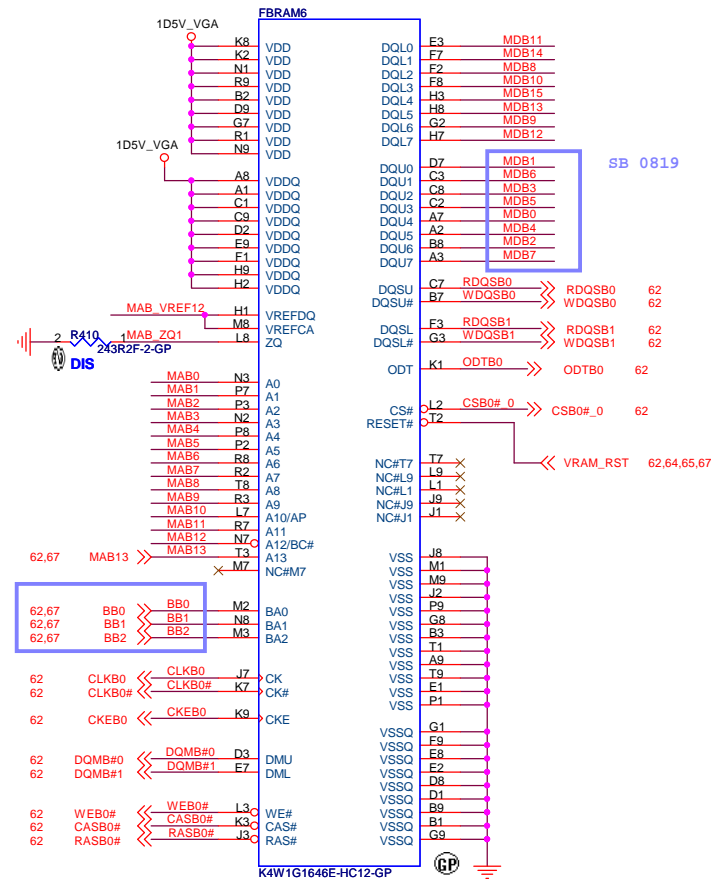
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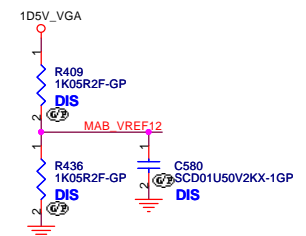
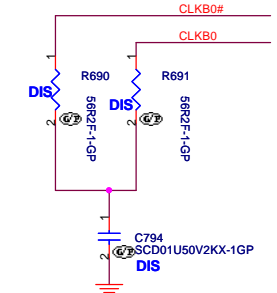
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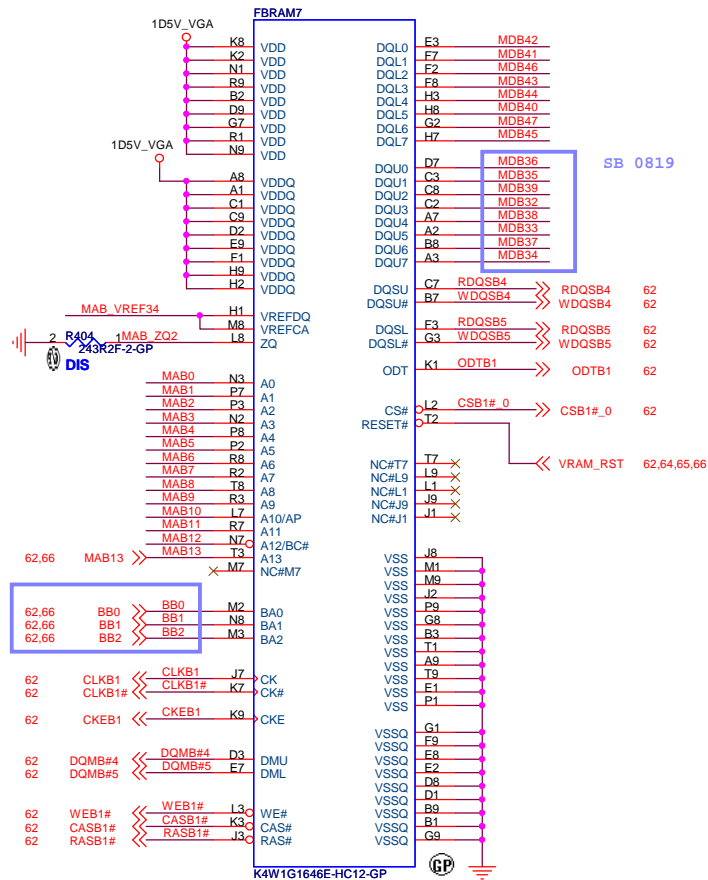
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# DDR3



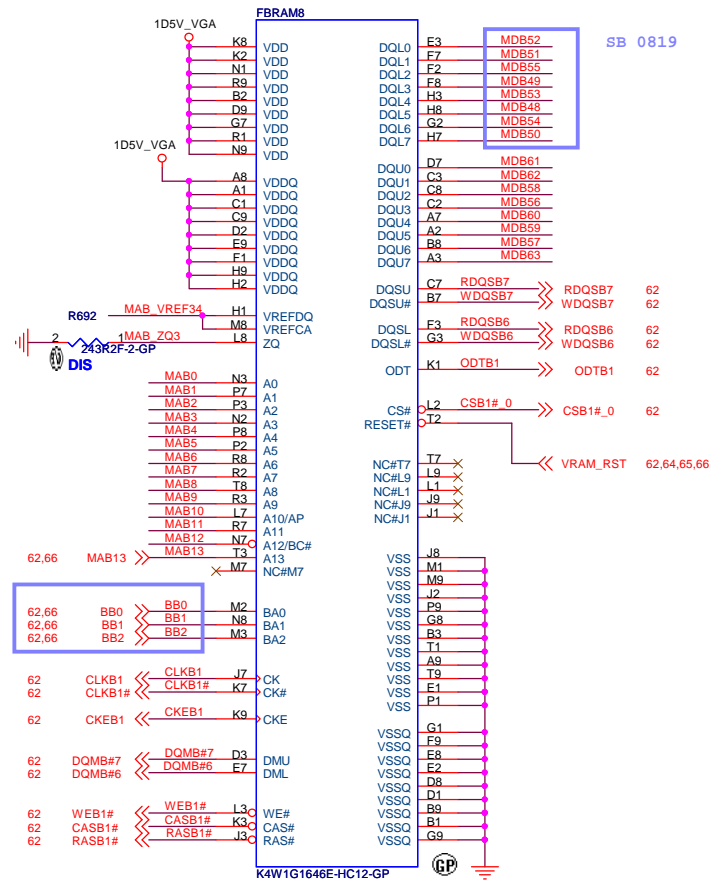
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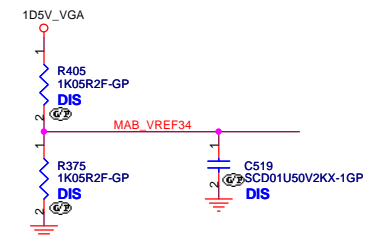
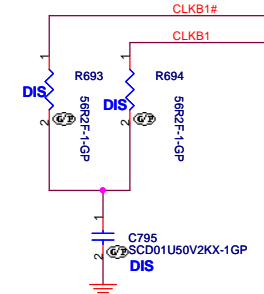
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72.41164.H0U

**HYN-72.51G63.C0U,SAM-72.41164.H0U**

DIS



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|                                  |                 |    |           |
|----------------------------------|-----------------|----|-----------|
| Title                            |                 |    |           |
| <b>VRAM(4/4)</b>                 |                 |    |           |
| Size<br>A3                       | Document Number |    | Rev<br>-1 |
| <b>JV70-CP</b>                   |                 |    |           |
| Date: Thursday, October 08, 2009 | Sheet 67        | of | 68        |

|   |   |   |   |   |   |
|---|---|---|---|---|---|
|   | 5 | 4 | 3 | 2 | 1 |
| D |   |   |   |   |   |
| C |   |   |   |   |   |
| B |   |   |   |   |   |
| A |   |   |   |   |   |

JV70-CP

|                       |                            |   |                |
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| Title                 |                            |   |                |
| <b>Modify History</b> |                            |   |                |
| Size                  | Document Number            |   | Rev            |
|                       | <b>JV70-CP</b>             |   | <b>-1</b>      |
| Date:                 | Thursday, October 08, 2009 |   | Sheet 68 of 68 |